Inventronik GmbH.
Kompetente Lösungen für Ihre Ideen

Finkenstraße 48
70199 Stuttgart

Tel: +49 - (0)711 - 60 19 637
FAX: +49 - (0)711 - 60 19 638
Mail: post@inventronik.de
Internet: www.inventronik.de

Viplax

Users Manual

Viplax Transmitter- / Receiver Unit

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History

Issue	*Date*	*Reason For Changes*
01	20040517	Initial issue
02	20040603	Added Schematics and PCBs.

References

[1]

Introduction

Ladies and Gentlemen,

Thank you for purchasing Viplax from Inventronik GmbH. With the purchase of this product you have acquired a high-quality Analog-Signal transportation system. Please read this user manual completely before start-up. This document will give you comprehensive information regarding Viplax capabilities and how you can most efficently use them. Inventronik GmbH is endeavored to keep the most current information concerning our products at your disposal. On our website (www.inventronik.de) the newest documents are available for you to download.

Safety Restrictions

Inventronik GmbH is proud to supply you with a high-quality device, nevertheless we cannot guarantee that this module works under all possible conditions without failure. Do not use this product in applications, where damage in the module could lead to direct danger for humans, e.g. medical systems, protection devices and such.

Inventronik GmbH cannot be held in any way responsible for general or specific damages caused by abuse or misuse of our products.

This product is conceived exclusively for use with the specified voltages. We recommend the use of the Viplax power supply. Higher voltages can lead to malfunction and/or the total loss of the module. **Please only use certified power supplies.**

General Description of the Viplax Transmission System

Viplax is a system designed for transmitting analog bipolar signals with little regard to the difference in electrical potential. Electrical isolation has been accomplished by using a fiber optic line between transmitter and receiver. The analog input signal on one end is converted to a digital signal, serialized and sent via highspeed fiber optic link to the receiver unit.

The receiver unit reverses the process, converting the serial data with mimimal delay and extreme accuracy back into the analog signal measured by the transmitter.

A high-quality, low-impedance output-driver delivers the recovered analog signal to loads with small impedance e.g. correctly terminated coaxial cables at 50 or 75 Ohm. The digital resolution of the system is 14 bit. The analog bandwidth lies at about 2.5MHz (3dB).

Besides the analog data transmission there are additional features distinguishing Viplax from other commercial systems. For instance, digital data processing, fast and accurate comparator functions, comfortable software, easy offset calibration, and support for software or hardware add-ons.

For further information regarding these additional features please refer to the dedicated chapters in this document.

Shipping List

A standard set of Viplax transmission systems consists of the following components:

- A transmitter unit: Viplax Transmitter.
- A power supply.
- A fiber optic line with a length of 2m (other lengths are available on request).
- A receiver unit.
- For configuration: a 1 meter USB or TCP/IP cable (depending on the type of receiver).
- CD-Rom with datasheets, circuit diagrams, documentation and system software.

Accessories

Currently available accessories for Viplax:

- Power supply for the receiver: 3U, 14HU plug in unit for 19“ rack mount systems.
- Fiber optic links: custom lengths
- USB or TCP/IP interface cables in several lengths.
- Backplane Basic: backplane for 19 inch 3U systems. This printed circuit board wires a Viplax receiver power supply with one receiver.
- Backplane Basic-Bi: backplane für 19 inch 3U systems. This printed circuit board wires a Viplax receiver power supply with two receivers.

If you have need of special equipment please contact Inventronik GmbH (www.inventronik.de).

Viplax Transmitter

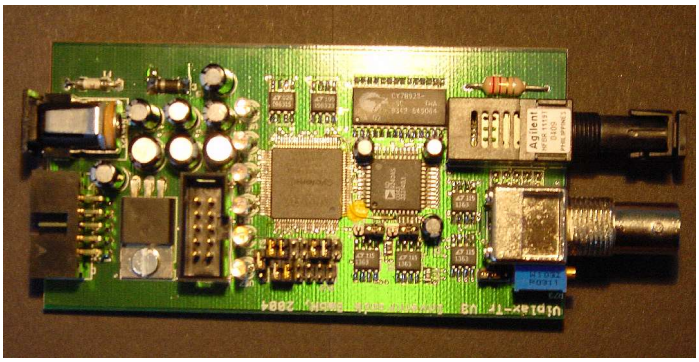


figure 1: Viplax Transmitter (handheld version).

Technical Description

The Viplax transmitter has two different case options. The a 3U unit is for 19" rack-mount systems and the compact, high frequency resistant, metal case, is suited for high voltage applications. There are only a few adjustments, and three cables necessary to operate the transmitter unit. The following description is specifically for the handheld version, but the 3U 19" version operates the same way, except the power supply is connected via a backplane Basic or Basic-Bi.

The transmitter is a powerful unit, compact, easy-to-install and maintenance free thanks to the use of modern electronic components. It's main elements are; a high quality analog digital converter with high resolution, a modern Field Programmable Gate Array (FPGA), a high-speed bitstream converter and a high-speed optical transmitter unit.

The data processing in the transmitter unit functions as follows: a BNC or SMB-jack connects the analog input signal. One or the other is available for the handheld unit, both for the rack mount version. An input amplifier with 1MOhm input impedance has gain factors of 1.0; 2.5; 4.0; 10.0 and 40.0. Two other gain factors are individually setable by adding components to the circuit board. The selection of the desired gain factor is done via jumper (figure 2).

To avoid signal distortion through aliasing effects there is a 'Bessel' filter of 4^{th} order (24dB/octave) between the preamplifier and the analog digital converter. In the attachment you will find some simulation plots of this unit.

The AD converter has a resolution of 14bit and a sampling rate of 10MSps transmiting analog signals with a bandwidth of 2.5MHz.

In addition to the AD payload there are four system check bits to transmit. The status of the power supply, the AD converter overflow bit, the comparator status and a freely usable FLAG „GP_BIT7“, which is connected to pin 9 of the auxiliary port.

Finally all parallel digital data are serialized, transmission check bits are generated and send through high speed optical link.

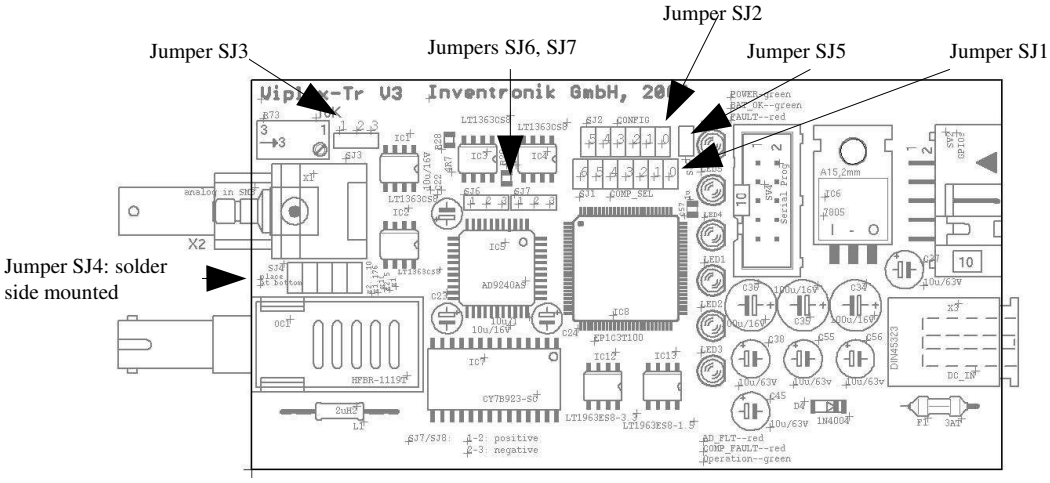


figure 2: Viplax Transmitter: Jumpers for gain and polarity adjustments.

Adjustment of the gain factor

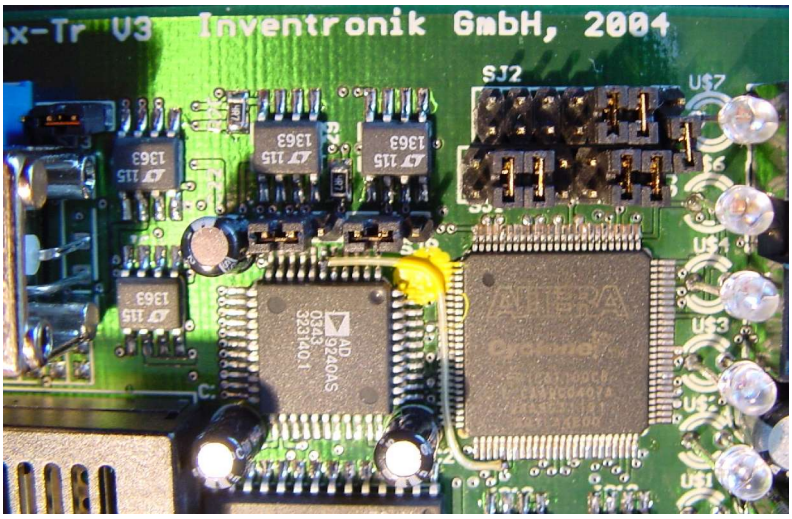


figure 3: Configuration of the Viplax Transmitter via Jumpers.

figure 2, 3 and figure 4 show the configurable jumper fields for gain adjustments. The first step is to disassemble the circuit board from it's case.

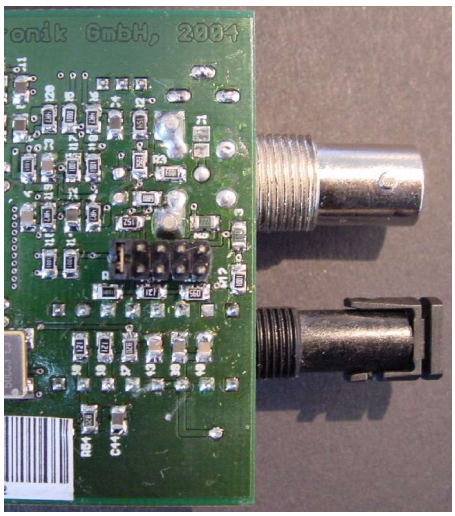


figure 4: Konfiguration of the gain factor.

The disassembly is shown in figure 5. Remove the cap which covers the BNC/SMB jack and the ST jack on the left side of the fiber optic transmitter.

Attention: the only way to remove the circuit board from the handheld case is as shown in the figure below. ***Do not try to remove the board from the right side of the case!*** This may damage either the case or the circuit board.

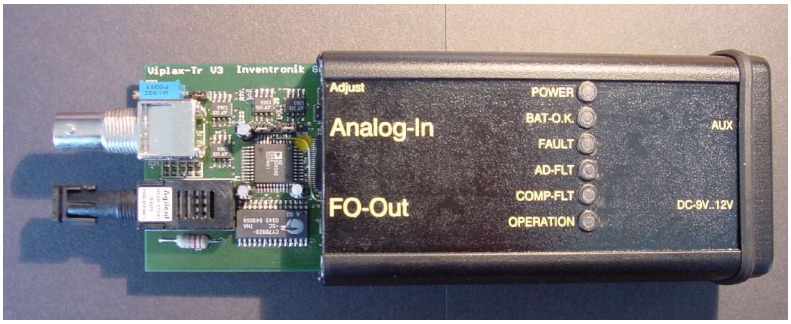


figure 5: Disassembly of the transmitter PCB to the left side!

The gain *v* of the preamplifier has to be calculated as the product of the adjustments of the jumpers SJ3 and SJ4 (see figures 3 and 4). In rows 5 and 6 of table 1 the gain factors of the Viplax system (transmitter-receiver) are referenced to the analog outputs (BNC/SMB) of the receiver.

The output, connected to the BNC jack has a maximum amplitude of +/- 5V, and the SMB jack has an amplitude of +/- 10V. The different gain factors are adjustable as follows:

SJ3:	*1-2*	*2-3*	*1-2*	*2-3*	*1-2*	*2-3*	*1-2*	*2-3*	*1-2*	*2-3*
SJ4:	*x1*	*x1*	*x2.5*	*x2.5*	*x10*	*x10*	*x2..10*	*x2..10*	*ud**	*ud**
U_{inmax}	*±10V*	*±2.5V*	*±4V*	*±1V*	*±1V*	*±0.25V*	*±5..1V*	*±1.25..0.25V*	-	-
v	0.25	1.0	0.625	2.5	2.5	10.0	0.5..2.5	2..10	-	-
U_{in} / U_{BNC}	0.5	2.0	1.25	5.0	5.0	20.0	1...5	4...20	-	-
U_{in} / U_{SMB}	1.0	4.0	2.5	10.0	10.0	40.0	2...10	8...80	-	-

table 1: selectable gain factors and the resulting total gain v over the maximum input voltage. (*ud – user defined gain).

It is not recommended to select the gain combination marked grey in table 1. The total gain v is more accurately achieved by other combinations. Further information on the user selectable gain factors can be found in technical data section of this handbook.

If user selectable factors are desired, fine tuning can be achieved by a potentiometer which is located directly behind the left panel on the right side of the BNC- respective the SMB jack.

Adjustment of the Amplifier Polarity

Jumper SJ6 and SJ7 puts the transmitter input amplifier into inverted or non-inverted operation. Both jumpers located in position 1-2 (figure 2, 1-2: jumper are in left position), the amplifier works non-inverting mode. Inverted mode is activated by putting both jumpers to position 2-3. Both jumpers must be located either in position 1-2 or in position 2-3. A mixed positioning is not valid and leads to malfunction.

Adjustment of the Window Comparators of the Transmitter

The absolute value of the comparator threshold is configured through jumper block SJ1 (figures 2 and 3). Adjustment of the threshold is achieved in steps of 1% (based on maximum value). Using the jumper block as 7bit binary, you need to encode the desired value. An installed jumper „x“ means a logic '1' and a not installed jumper „-“ a logic '0'.
Example: A threshold of 67% = x----xx (100011 = decimal 67).
The LSB (least significant bit) is located to the right. Since there is a maximum of 127% adjustable, all values greater 100% are interpreted as 100%. The threshold value may be used for positive and negative comparator values. A threshold setting of 100% equals an input signal of exactly 2.5V (absolute value). This means that the preamplified input signal may not exceed this value not to produce AD converter overflow or wrong comparator behaviour. With the jumper block SJ2 there are negative, positive or both comparators selectable (table 2).

Using the two least significant bits of SJ2 jumper will adjust the transmitter comparators (table 2); (not installed jumper: „-“; installed jumper „x“; don't care: „.“)

SJ2	***Description***
....xx	Comparator detects overstepping of positive and negative thresholds.
....x-	Comparator detects overstepping of positive thresholds only.
....-x	Comparator detects overstepping of negative thresholds only.
....--	Factory setting; no comparator active

table 2: Adjustment of the comparator functionality via SJ2.

The comparator is active, if jumper SJ5 is inserted otherwise deactivated.

The factory setting of the comparators is inactive due to missing SJ5. Transmitter comparators are helpful if you want to supervise the input signal directly at the transmitter case. Otherwise we recommend to use the more powerful receiver comparators. These comparators are more powerful and allow easy adjustment through PC integration.

Default Jumper Settings:

The transmitter factory settings for the jumpers SJ1 to SJ7:

Jumper:	***Adjustment***	***Remarks***
SJ1	-xx--x-	50,00%
SJ2	----xx	both, positive and negative supervision
SJ3	position 2-3	prescaler adjusted to factor 1.0
SJ4	x1	gain set to factor 1
SJ5	open	comparator inactive
SJ6	1-2	non-inverting operation
SJ7	1-2	non-inverting operation

table 3: Factory transmitter jumper settings.

Visualisation

Six LEDs are located on the top cover of Viplax transmitter (handheld version). All LEDs are used for status and error indication:

1. POWER: power status. This LED indicates the correct function of the internal charge pump. The charge pump is used to create the negative voltage supply. The LED may be darker than the other to avoid unnecessary load of the charge pump.
2. BAT-O.K.: voltage supervision control. You may use a battery to power the Viplax transmitter. This LED detects its correct charge condition. If the transmitter is operated by a power supply, the LED statically is turned on.
3. FAULT: collective error. It indicates either a comparator threshold or an AD converter overflow error.
4. AD-FLT: overflow error of the AD converter. This LED indicates if the AD converter is driven into saturation by too high input signals. Solution is to reduce the input voltage or the amplification factor.
5. COMP-FLT: comparator threshold event. The LED indicates the input voltage falls outside of the adjusted thresholds.
6. OPERATION: indicates steady operation, a well initialized transmitter without system faults or other errors (no comparator- or AD converter errors and battery in good charge condition).

Auxiliary Port

The Viplax transmitter unit is equipped with an auxiliary port that carries the 5V operating voltage, GND and eight user defined input/output lines. This port has the factory setting except pin 9 „GP_BIT7“ which is inactive. It is dedicated for system enhancements (please contact Inventronik GmbH for usage). The port connector is a 90-degree 10-pin header in 0.1 inch form factor. It is located right behind the right panel (figure 2).

Power supply

The power supply with 9V...12V DC is used to power the Viplax transmitter (part of the delivery). The recommended setting is 9V.

The polarity of the power supply connector is minus on the inner rod and plus on the outer contact.

The transmitter provides an optimized voltage control system to ease the use of a backup battery. Supervision of the battery charge condition is accomplished by a comparator. This status information is also available to the receiver unit.

The delivered power supply is build in 50Hz technique. **We do not recommend other power supplies such as switched mode power supplies. The usage of these modern supplies may reduce the analog signal quality dramatically!**

The layout of the drills of the of the original power supply is given in figure 6.

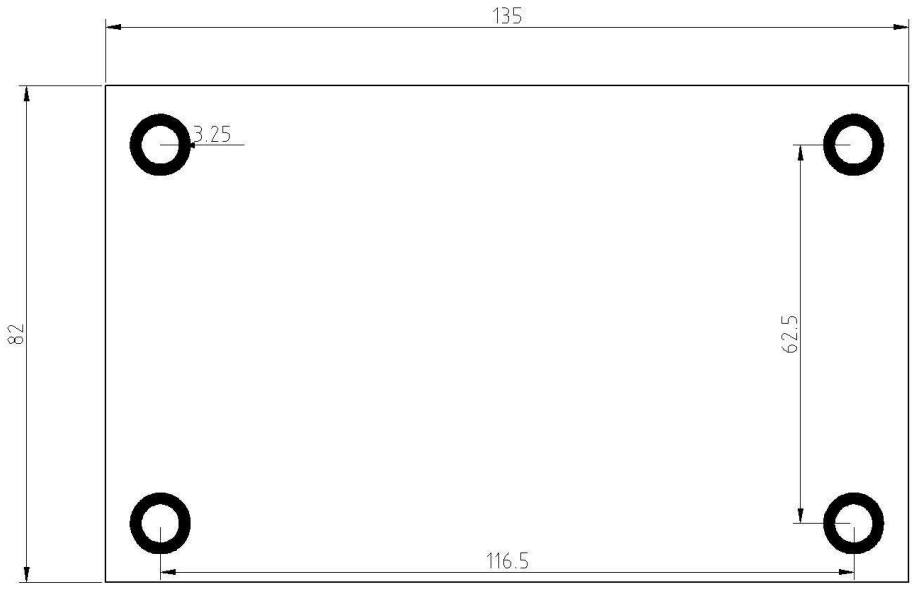


figure 6: mechanical Layout of the stand alone transmitter power supply

Maintenance of the Transmitter

Under normal circumstances the Viplax transmitter requires no maintenance. Merely, if the supply voltage polarity has been connected in a wrong way, it is possible that the transmitters internal fuse got blown and must be replaced. The fuse is the F1 on the PCB (PicoFuse). See also the layouts in the attachment to this document.

If the transmitter is not connected to a fiber optic line, a cap should protect the optical subsystem to avoid any damage.

Do not touch the fiber optic connector at its 'Ferrule'. If Viplax is not used, please cover the Ferrules with a dust caps.

Viplax Receiver

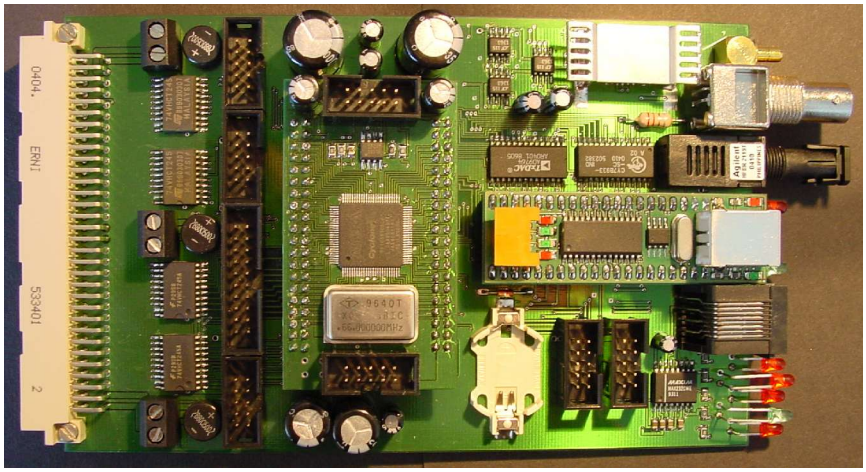


figure 7 : Viplax Receiver.

Technical Description

Digital data processing goes vice versa, compared to the transmitter. The received serial data stream will be converted into parallel equivalent. Transmission check bits indicate a valid reception. Next the system check bits and the user-bit GP_BIT7 are extracted (see attachments: connector X6 pin number 8, (D_OUT1).

The remaining parallel data is converted back to an analog signal. Two output amplifiers provide the desired output signal conditioning. The analog output is available on two output connectors. The first output is capable to drive 50 Ohm loads (BNC jack) and the other one 75 Ohm loads (SM jack). The maximum output voltage swing is +/-5V at 50Ω and +/-10V at 75Ω.

Viplax receivers are equipped with a microcontroller system board which provides the control and supervision of the digital data processing. Communication with a host computer is available through a USB- or TCP/IP ethernet interface (depending on the type of the Viplax receiver).

The highspeed digital data processing is implemented in a field programmable gate aray (FPGA), which is a custom design.

Both, the microcontroller unit and the FPGA unit are separate modules pluggable to the Viplax system board. The microcontroller unit is either a MiniFlex-USB module (USB version) or a ARM7TDMI embedded Linux (TCP/IP version) from FS-Forth Systems. The FPGA is a Sphinx-C100-RevA2 module. Further informations can be found in the chapters concerning the software configuration.

The receiver comes in euroboard form factor. All digital signals are connected to headers and/or 64 pin (a+c) VG type connector. The printed circuit board is installed in a 3U, 10HU plug-in case.

Functional Description of the Error Logic

Viplax includes a fast error detection logic with a total response time of about 1,5µs (inclusive data transmission from the transmitter to the receiver). This system exists of two separate subsystems, the **error processing system** and the **first fault memory**.

Error Processing System

Transmitter and receiver errors will be collected and processed by this instance. The error processing system is optimized and needs only several system clock cycles (about 100ns). Compared to the total response time, the error handling is almost negligible.
The description of the error system behaviour and the resulting system status is described as follows. All signals are 'active high':

- **LOW_BAT:** This error signal is caused by the transmitter. The signal is connected to the output D_OUT2 (connector X6, pin 7). It is also an input to the first fault memory.
- **COMP_FLT:** This error signal is caused by the transmitter. The signal is connected to the output D_OUT3 (connector X6, pin 6). It is also an input to the first fault memory.
- **AD_FLT:** This error signal is caused by the transmitter. The signal is connected to the output D_OUT4 (connector X6, pin 5). It is also an input to the first fault memory.
- **LINK_FLT:** This signal indicates a fiber optic error. It is asserted in case of a not installed or or faulty fiber optic cable. Other reasons are the damage of the optical subsystem in transmitter or receiver component. A LED on the front panel will indicate this error. Furthermore it is an input to the first fault memory and, in combination with the enable status of the microprocessor, connected as LINK_RDY to D_OUT5 (connector X6, pin4).
- **LINK_RDY**: This status indicates the standby of the Viplax transmission system. LINK_RDY is deasserted if a LINK_FLT is asserted or if the microcontroller is in configuration process e.g. changing comparator thresholds to the FPGA. Right after power up or after a system reset, the signal is suppressed for about 300ms to guarantee the correct initialisation of the internal phase locked loop circuits. The signal is connected to the output D_OUT5 (connector X6, pin 4).
- **COMP_1L, COMP_1H, COMP_2L, COMP_2H:** are the upper respective lower thresholds of the both receiver comparator units. These signals are not connected to any outputs but used as inputs to the first fault memory.

If desired, the error detection system can be disabled. However this has also an effect to the first fault memory, since these errors are not available anymore.
The only exception is the LINK_FLT signal which is always enabled to guarantee a reliable supervision of the fiber optic line.

figure 8 : Viplax Receiver (front view).

First Fault Memory

The First Fault Memory sub-system is responsible for storing errors. If an error occurs there might be a lot of consecutive errors as result of the initial fault. Since these consecutive errors are just a side effect the system masks them out. Only the first fault is stored.
There is one exception. The LINK_FLT error is stored in any case. In principle it is possible that more than one error is stored in the memory if they occur exactly at the same time. The first fault memory is available until erased by the user. Erasing the first fault memory is achieved by the service software (see below) or by asserting a TTL signal to the digital input D_IN6 (pin A25 of the 64 pin VG type connector X5). The service software allows erasing the first fault memory periodically.

The first fault memory generates the following error signals:

COMP_1L, COMP_1H, COMP_2L, COMP_2H, LOW_BAT, AD_FLT, COMP_FAULT and LINK_FLT.

The two last mentioned signals have a special function.

The COMP_FAULT is a collective error of the transmitter and receiver comparator thresholds.

A fault in the fiber optics occurs right after power up sequence or after a system reset. Responsible for this behaviour are the inrush effects of the built in phase locked loops. For this reason the LINK_FLT memory is disabled for about 300ms during power up or reset.

All memories except the LINK_FLT can be disabled or enabled via the service software.

The memory locations are wired to the connector X5 (64 pin VG type connector) according to the following table.

Signal	*connector pin of X5*
LINK_FLT	A16
COMP_1L	A17
COMP_1H	A18
COMP_2L	A19
COMP_2H	A20
COMP_FAULT	A21
LOW_BAT	A22
AD_FLT	A23

table 4: Error Signals wired to the connector X5.

Additionally the signals are wired to the 10 pin header X10 according to the following table:

Signal	*connector pin of X10*	*Signal*	*connector pin of X10*
COMP1_L	PIN1	COMP1_H	PIN2
COMP2_L	PIN3	COMP2_H	PIN4
LINK_FLT	PIN5	LOW_BAT	PIN6
AD_FLT	PIN7	COMP_FAULT	PIN8
GND	PIN9	GND	PIN10

table 5: Error Signals wired to the connector X10.

Signal LEDs

The Viplax receiver with USB has 7 LEDs (figure 8). The LEDs are described as follows:

LINK-FLT	There is trouble with the fiber optics.
STDBY	The Viplax transmission system is in standby and ready to operate.
AD-FLT	The first fault was an AD_FLT .
LOW-BAT	The first fault was a LOW_BAT.
COMP-FLT	The first fault was a COMP_FLT .
USB-TxD	USB send signal
USB-RxD	USB receive signal

table 6: Signalisation of the USB type.

The Viplax receiver with TCP/IP has 8 LEDs. The LEDs are described in the following table.

STDBY	The Viplax transmission system is in standby and ready to operate.
LINK-FLT	There is trouble with the fiber optics.
AD-FLT	The first fault was an AD_FLT .
LOW-BAT	The first fault was a LOW_BAT.
COMP-FLT	The first fault was a COMP_FLT .
ACTIVITY	There is data transfer activity in the ethernet.
STATUS 1	Not used so far.
STATUS 2	Not used so far.

table 7: Signalisation of the TCP/IP type.

Digital Interface

The Viplax receiver does not only convert the received serial data stream into an analog output signal, it also provides a parallel TTL conform digital interface for the analog data at connector X5. This option allows to do real time data processing.

The used 14bit data format is defines as:

A binary '0' („00000000000000“) represents -100% of the analog value,
a „10000000000000“ represents 0% and
a „11111111111111“ +100% of the analog value.

Additionally there is a control signal 'DA_D_VALID' , which indicates by its logic '1' state, that the data is valid.
The signal 'DA_D_VALID' is asserted only in the case that no transmitter error is detected ('AD_FLT' or 'LOW_BAT') and the fiber optics work fine. As soon as a 'LINK_FLT' occurs, digital data is not valid indicated by 'DA_D_VALID' = 0. In this case the digital data itself will be set to „10000000000000“.
If the data processing system is disabled DA_D_VALID will be asserted even in the case, when there are transmitter errors detected ('AD_FLT', 'LOW_BAT'). The table below shows the connector pinout for X5.

All signal are TTL compatible. The 14bit digital analog data is defined by DA_D13 downto DA_D0 where DA_D13 is the most significant bit and DA_D0 the least significant one.

Connector Pin	*Signal*	*Connector Pin*	*Signal*
X5-A1	*DA_D13*	*X5-A9*	*DA_D5*
X5-A2	*DA_D12*	X5-A10	*DA_D4*
X5-A3	*DA_D11*	X5-A11	*DA_D3*
X5-A4	*DA_D10*	X5-A12	*DA_D2*
X5-A5	*DA_D9*	X5-A13	*DA_D1*
X5-A6	*DA_D8*	X5-A14	*DA_D0*
X5-A7	*DA_D7*	X5-A15	*DA_D_VALID*
X5-A8	*DA_D6*		

table 8: Digital Data wired to the connector X5.

Additionally the connector X11 is wired with the digital data and with the status information 'AD_FLT' of the first fault memory. Table 9 shows the connector layout.

Connector Pin	*Signal*	*Connector Pin*	*Signal*
X11-PIN3	*DA_D13*	*X11-PIN11*	*DA_D5*
X11-PIN4	*DA_D12*	X11-PIN12	*DA_D4*
X11-PIN5	*DA_D11*	X11-PIN13	*DA_D3*
X11-PIN6	*DA_D10*	X11-PIN14	*DA_D2*
X11-PIN7	*DA_D9*	X11-PIN15	*DA_D1*
X11-PIN8	*DA_D8*	X11-PIN16	*DA_D0*
X11-PIN9	*DA_D7*	X11-PIN17	*DA_D_VALID*
X11-PIN10	*DA_D6*	X11-PIN18	AD_FLT

Table 9: Digital Interface wired to connector X11.

Digital I/O-Ports

In the preceding chapters, most of the digital signals are explained. Mentioned but not described up to now is the RESETn which is wired to D_OUT6 respective to the connector X6 pin number 3. The signal is also connected to the reset push button, which is located behind the small hole of the front panel and is low active. D_OUT6 can be used to initialize peripheral components together with the Viplax transmission system.

A collection of all connector layouts can be found in the appendix of this document.

Power Supply for the Receiver

The receiver requires three different voltages. Two times 15 VAC / 250mA and 9VAC / 1.4A. Inventronik GmbH has a suitable power supply in its portfolio.

The supply for the receiver can be connected to the 64 pin VG type connector or to clamps located behind the VG connector. Last mentioned are to the best advantage if the receiver shall not be mounted in a 19“ rack, but used as a stand alone component. In this case the rear panel of the plug-in unit has to be removed to gain access to the clamps. The layout of the receiver (see appendix) or figure 7 shows the position of the clamps in detail. The connector X5 connects to the power supplies as follows:

Connector Pin	***Signal***
X5-C1	*15V AC I*
X5-C2	*15V AC I*
X5-C16	*9V AC*
X5-C17	*9V AC*
X5-C31	15V AC II
X5-C32	15V AC II

Table 10: Supply voltages for the receiver connected via connector X5.

Power Up Sequence

The power up sequence of the Viplax transmission system is not critical. It doesn't matter in which order the transmitter and the receiver are powered on. Merely there is the effect, that the LINK_FLT is suppressed for 300ms due to the phase locked loops as mentioned above. Is the link after 300ms not established, the LINK_FLT can not be cleared. After clearing the faults by a reset or by the service software, the Viplax transmission system is ready to use.

Maintenance of the Receiver

The Viplax receiver is completely maintenance free. Take care of the very sensitive fiber optics.

If the receiver is not connected to a fiber optic line, a cap should protect the optical subsystem to avoid any damage.

Do not touch the fiber optic connector at its 'Ferrule'. If Viplax is not used, please cover the Ferrules with dust caps.

Maintenance of the Transmission System

The Viplax transmission system is nearly free of maintenance except of long term offset re-calibrations. Ageing of components over the time may make this necessary. The user can independently calibrate the offset values of transmitter A/D converter and the receiver D/A converter via the system software.

Offset Calibration

Prerequisites for the calibration of the Viplax transmission system is a high quality multimeter and a 50Ω BNC-terminator for the BNC type transmitter or a suitable SMB terminator with 50Ω (a SMB-short circuit connector will do it too). The calibration should be accomplished on equipment with operating temperature. An operation of one hour before starting the calibration process is recommended.

First step is connecting the multimeter (DC voltage measurement) to the receivers BNC jack. The receiver calibration is done with disconnected fiber optic, i. e. with asserted LINK_FLT. To adjust the offset of the receiver it is necessary to start the service program. The offset calibration is very simple. The measured offset has to be minimized with the software receiver calibration buttons.

In a next step, a terminator must be installed at the transmitter and the fiber optic link has to be established. The LINK_FLT needs to be cleared by the service software. Now the Viplax transmission system should be in operation condition. To minimize the offset use again the software calibration buttons, but this time for the transmitter.

Viplax is adjustable to a minimum offset of about 1mV. An optimal 0.0mV offset is not possible due to noise, the relative simple offset calibration equipment and also due to the finite quantisation of the AD- and DA converters.

Viplax Service-Software

Viplax Interface Options

There are two options to establish communication between PC and the Viplax receiver. The USB interface is useful if the Viplax receiver is nearby or if you have a notebook at your disposal. For long distance configuration we recommend the TCP/IP ethernet option. LANs are widely used and the necessary infrastructure normally allows for remote control of the Viplax receiver. The following sections will explain how to install the necessary device drivers and how to use the software.

USB Option: Installing a Driver for a Virtual USB/RS232 Port

The MiniFlex-USB needs to be connected with a power supply and the USB cable, after which you will be asked to select first a USB<->Serial driver and finally the USB-Serial-Port driver. You'll find these drivers on the product-CD in the directory Windows\USB Driver.

Why is this driver needed?

The driver maps the USB interface on your PC to a virtual serial RS-232-C interface. Programming a RS-232-C interface is much easier than programming the USB interface because you don't have to know about complicated USB protocols and you can use many well-tested programming libraries with serial communication support. Exchanging data via USB is really easy this way.

Please note: the driver version on the product is not certified by Windows XP (a warning appears).

Screenshots of the Installation Process

After connecting the MiniFlex-USB to your PC, a dialog window opens (see figure 4).

Figure 9: Windows hardware facility assistant

Don't use automatic installation here.

Please use the second option in the dialog window to allow selection of the appropriate directory. Press --- *WEITER*--- to continue.

The following dialog appears:

Figure 10: Selection of the driver directory

Please choose the location of the driver. You will find it on the product-CD in the folder (Windows\USB Driver). The installation procedure ends with the last dialog window. This will be the the „USB Serial Port“ installation. After that the virtual serial COM is ready for use.

Figure 11: Finish the driver installation; Serial converter

PCs are normally equipped with multiple COM-ports so the virtual COM-port is not mapped to a specific port number (e.g. COM3). Windows has its own scheme for the distribution of virtual port numbers. How to find the right COM port is discussed later in this documentation.

Figure 12: Finish the driver installation; USB serial port driver

Verifying the COM-Ports

Next you should find out which COM-port is used for the virtual serial interface. The COM-port in use depends on the number of COM-ports already available in your PC. To figure it out you'll have to open the device manager (system/hardware) and open connectors (COM and LPT). The USB Serial Port shows up (here COM4 is used for the USB Serial Port).

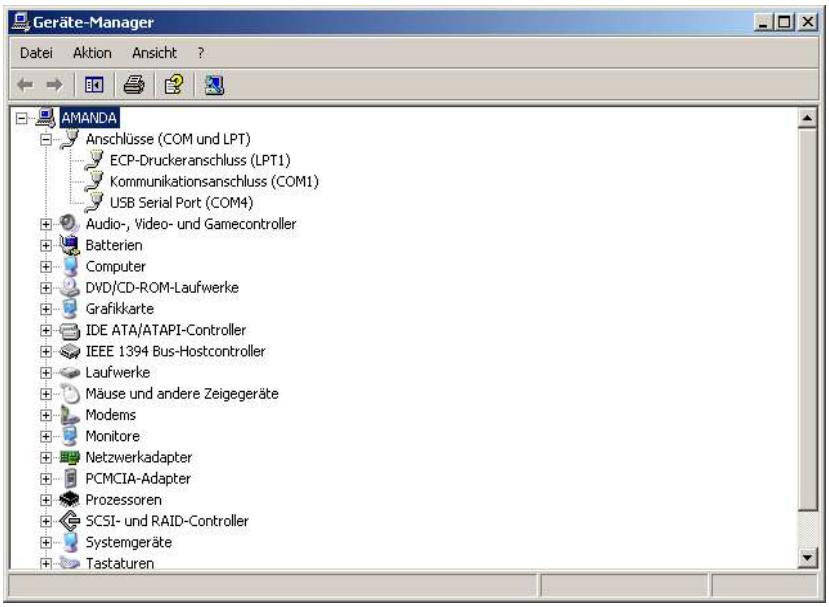


Figure 13: USB Serial Port (COMx)

Viplax Configuration Program

For the Windows 2000/XP™ operating system we offer an easy to use configuration program. All adjustments are spread over a tabbed form. The following screenshot shows what can be done.

1. ---*EINSTELLUNGEN*--- Choose a serial port:

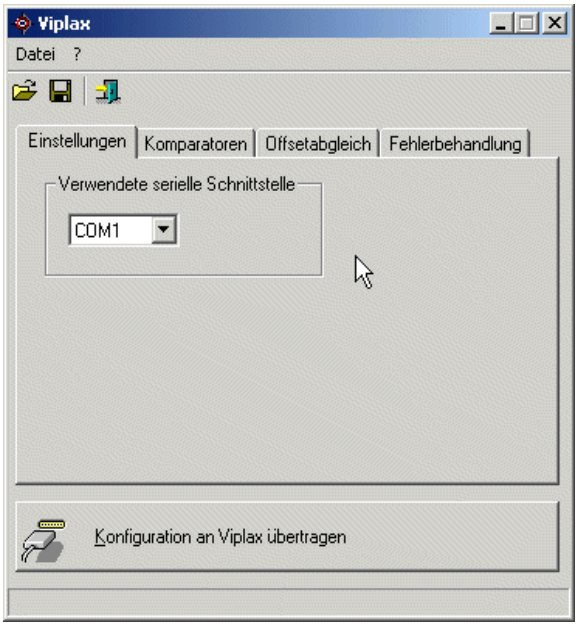


Figure 14: Viplax configuration program, serial interface

In this dialog form choose the virtual serial interface which you previously found to correspond with the used USB-port. Changes to the Viplax settings will not be transferred to the Viplax system until you click to the |--- *KONFIGURATION AN VIPLAX ÜBERTRAGEN*---| button.

2. ---*KOMPARATOREN*--- Adjustments to the threshold comparators:

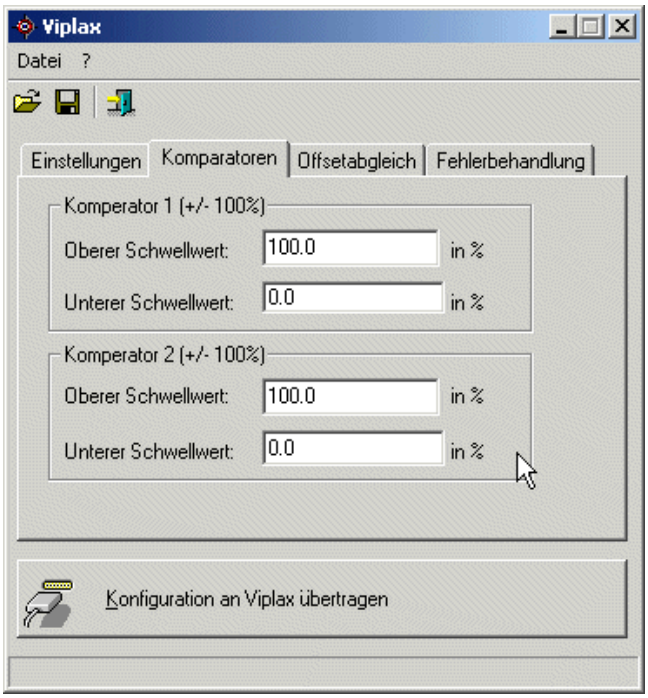


Figure 15: Viplax configuration program, thresholds

Input values are percentage values. Since we have a bipolar voltage input we extended the range and allow -100% to 100% values. Values in the range from 0% to 100% define a positive input threshold, -100% to 0% a negative one. The threshold comparator triggers an error if the input voltage falls below or raises above the adjusted thresholds.

3. ---*OFFSETABGLEICH*--- Adjustments for the 2nd threshold comparator: (see above)

4. ---*FEHLERBEHANDLUNG*--- Error handling:

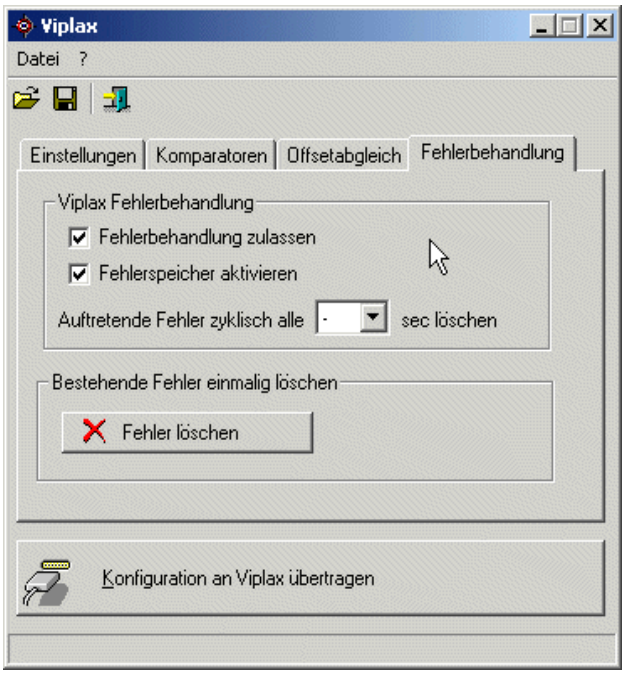


Figure 16: Viplax configuration program, error handling

The first checkbox enables or disables the general error handling.
The second one activates the first-fault-memory option.
If you want to erase upcoming errors in certain time cycles, you might use the cyclic error erase function ---*AUFTRETENDE FEHLER ZYKLISCH ALLE – SEC LÖSCHEN*--- '-' **disables** the cyclic error erase function.
The red error erase button ---*FEHLER LÖSCHEN*--- erases an error once.

5. ---*Offsetabgleich*--- Offset Values:

The offset adjustment can be done separately for the Viplax sender and receiver.

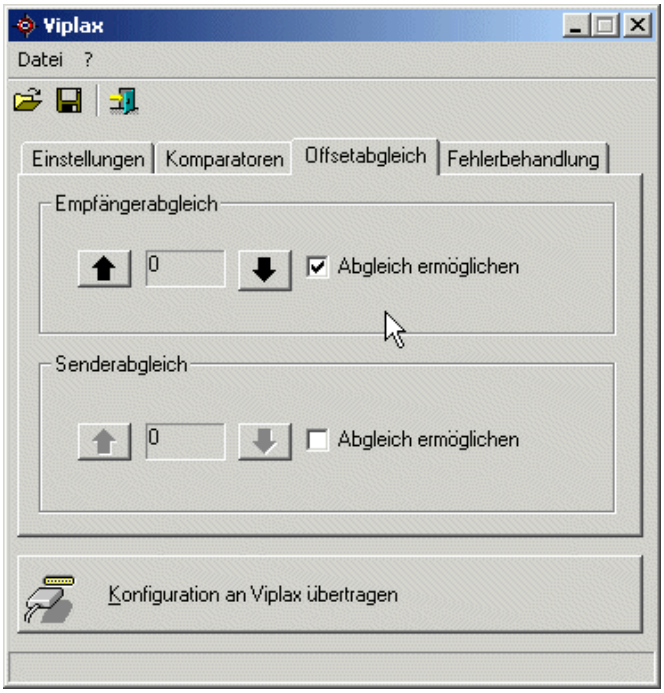


Figure 17:Viplax configuration program, offset adjustments

Each offset setting can take values between -127 and 128.
To change an offset value you have to enable the settings and use the up and down arrows. Normally it only takes small values to accomplish a satisfying offset calibration.
Please note: The ---*Konfiguration an Viplax übertragen*--- button is not necessary for the offset calibration! (See also Offset Calibration)

---*Konfiguration an Viplax übertragen*---
This button sends all adjustments to the Viplax receiver. If there is a problem with the serial port or if Viplax doesn't answer correctly you will get an error message.

If you need to integrate these Viplax functions into your own program, please let us know. We can provide information about the ASCII commands.

TCP/IP Ethernet-Interface: Using a Web-Browser for VIPLAX Configuration

Overview

A web server on the embedded Linux system in the Viplax receiver allows you to use a browser to adjust the various settings of Viplax. CGI-scripts provide basic authentication and allow easy configuration of the whole system.

Getting started

Before you power-on Viplax, you must establish a connection to your local network. A DHCP server is mandatory for the first start-up. This guarantees that Viplax can retrieve a valid IP address. Next you will need to know the assigned IP address to be able to make adjustments to your configuration with a web browser.

Resolving the IP address can be solved in different ways. One possibility is to log the boot process

with a serial RS-232-C monitor program on Viplaxs RS-232-C port. Use the Null-Modem-Cable (part of the Viplax shipping) to connect your PC with the Viplax serial port. Now, you have to start a monitor program. For Win32/XP you could use *HYPERTERM* which is part of Windows™. If you use Linux/Unix you might find *MINICOM* or *SEYON* helpful to monitor the boot messages. Please read also the man pages to those programs.

The serial port settings are as follows:

- Baudrate: 38400
- Databits: 8
- Stopbits: 1
- Parity: none

After a reset or after connecting Viplax to the power supply, you will get the following messages in your terminal program:

```
LxNETES Bootloader $Revision: 1.19 $

ABCDEFGHINO@00001618

Bootstrap: 03ff

...
```

after awhile the boot process stops and you will see a command line input prompt '#' (hash).

```
#
```

Now, if you scroll up the hyperterm output a bit, you will see following lines:

```
Sending DHCP requests ., OK

IP-Config: Got DHCP answer from DHCP-SERVER-ADDRESS, my address is
Viplax-IP-ADDRESS
```

Viplax-IP-ADDRESS is the IP address you will need to access the web frontend. Now open your favourite web browser and enter as URI: http://Viplax-IP-ADDRESS.

In our case we would type http://192.168.1.53

If you have administrator privileges on the DHCP server, you could look in the DHCP-log-files to figure out the assigned IP address, or if you are connected to a small local area network you might use *NMAP* to scan your network for new network devices. If nmap detects a device from FS-Forth it might be Viplax!

Viplax Start Page

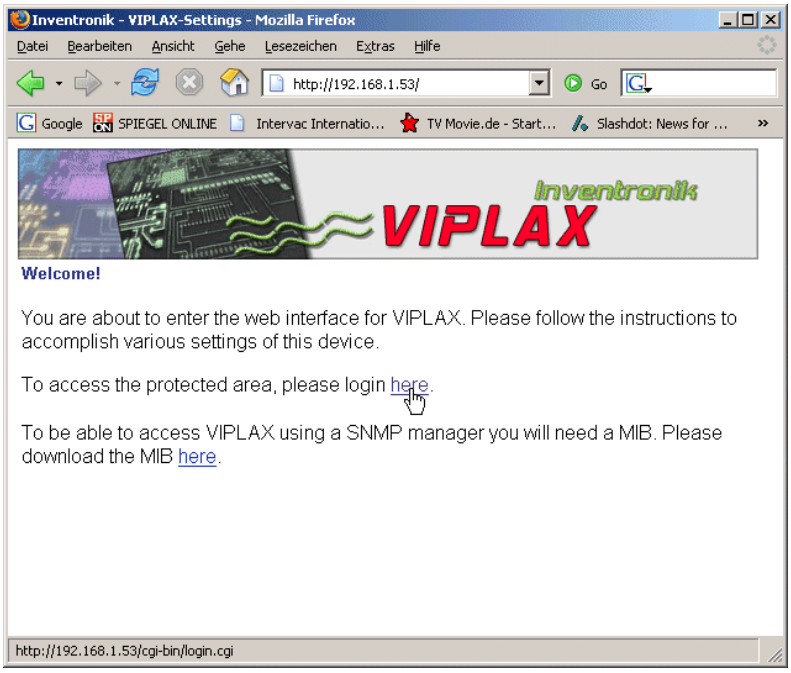


Figure 18:Welcome-Screen

Please use your favourite web-browser and follow the link *HERE* to be forwarded to the authentication page.

Viplax Login (HTTP-Authentication)

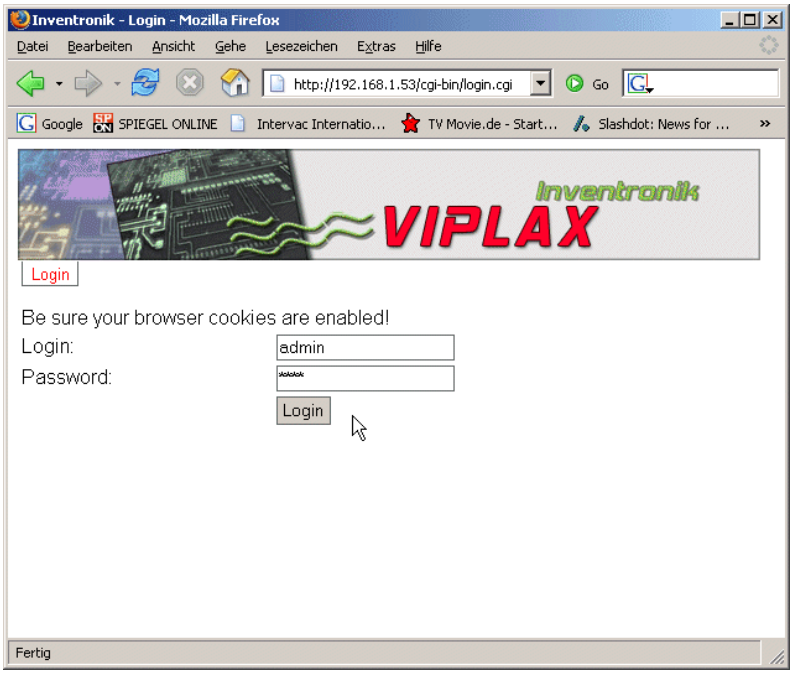


Figure 19: User Authentication

All Viplax functions are protected through authentication. You must login to be able to make any changes. To login successfully your browser cookies must be turned on!

First-time login is „**admin**“ and „**1234**“ is the default password. It is a good idea to change the password immediately after you have successfully logged-in.

If you can't login please confirm that your browser is accepting cookies.

Viplax Specific Adjustments

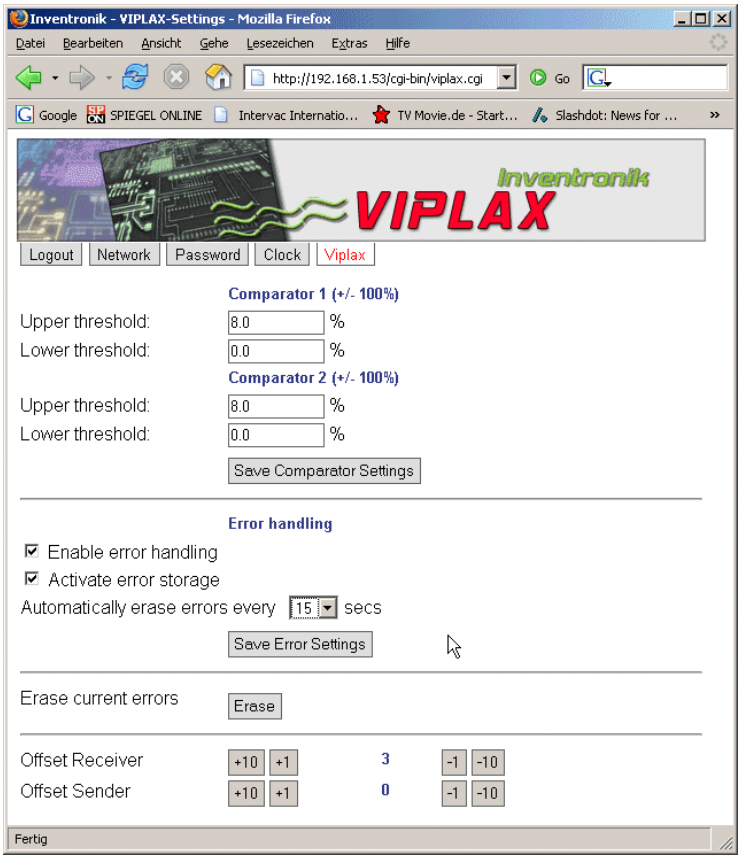


Figure 20: Viplax Adjustments

This figure shows all possible Viplax adjustments, which we have explained in detail in earlier sections of this manual.

- Adjusting the thresholds (see also ---Komparatoren--- Adjustments to the threshold comparators)
- Error handling (see also --- Fehlerbehandlung--- Error handling)
- Erase current errors.
- Offset adjustment (see also Offset Calibration)

Change Password

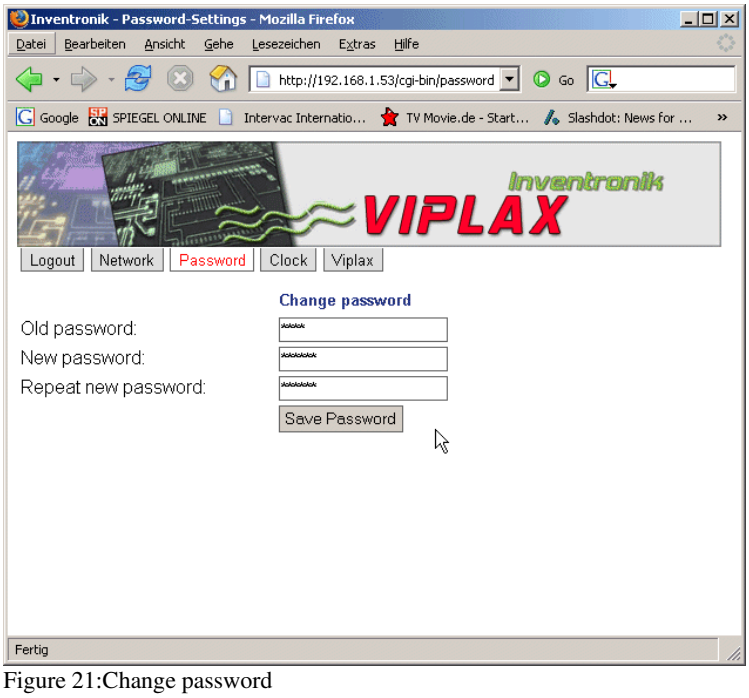


Figure 21:Change password

Not much to explain on this page! Anyhow, for security reasons it is necessary to type in your old password, then your new one and repeat.

In case you have forgotten your password, please email us and we will provide instructions on how to reset the password.

Network Settings

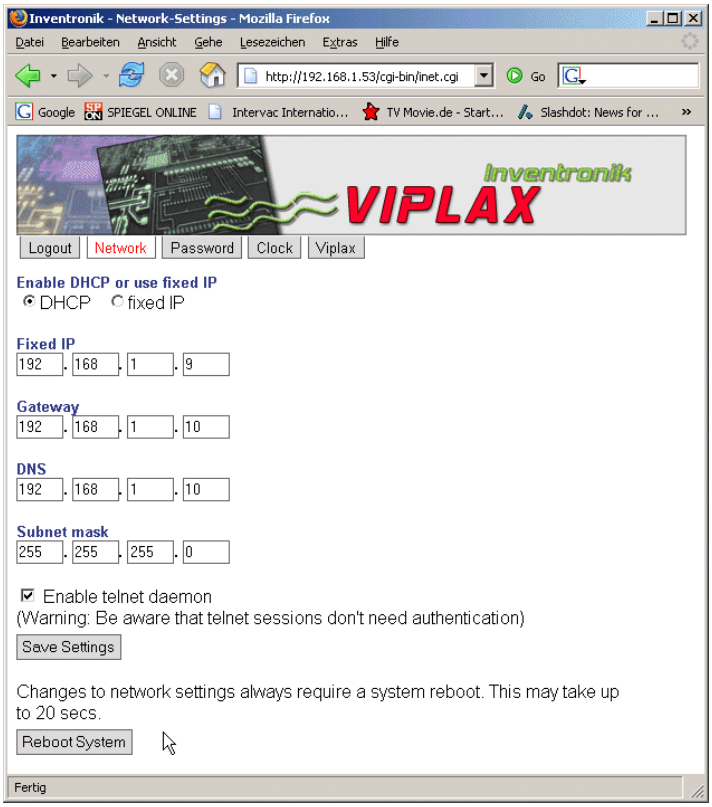


Figure 22: Viplax Network settings

Network integration with Viplax is easy. All adjustments can be made using the settings you see in the above screenshot. Predefined is the usage of a DHCP server. As mentioned earlier, to get things going, you need to have DHCP on the first time your boot your new Viplax. We recommend using a fixed IP address afterwards to avoid the Worst Case Scenerio or waiting for an unresponsive DHCP server (disconnected cable, unreachable DHCP server etc.)

Worst Case Scenerio: the DHCP server never answers and Viplax stays in an endless-loop stubbornly refusing start any services. Using a fixed IP avoids this!

The settings Gateway and DNS are not currently in use.

The telnet server enables remote sessions via TCP/IP. Once connected through a telnet client the user can reset some settings (e.g. passwords etc.). If you wish to use telnet please contact Inventronik GmbH. Do not use this option if you do not intend to access the system via telnet!

Please note: telnet sessions do not have authentication!

After changing any of the above settings, you must reboot the Viplax Linux system.

TCP/IP Protocol SNMP (Simple Network Management Protocol)

SNMP is widely used in a TCP/IP network, mostly for controlling of communication equipment. Since Viplax can be considered as a network device, we offer a SNMP interface to control Viplax.

Despite the fact that SNMP says it is a simple protocol, it is not easy to understand. We highly recommend that you checkout our link section for further readings.

Presumptions

SNMP applications are build as typical client/server applications. The client, also called Manager, is located on the controlling PC. The server, also called Agent, is ready to use on the Viplax-Receiver.

To be able to instantiate a communication path between manager and agent, you will need some basic programs on the controlling PC.

In our case we used the open source NET-SNMP (see http://net-snmp.org). The Viplax SNMP-agent uses the same software in version 5.2.1.

Viplax uses SNMP-Protocol V2 (but V3 should work too, but we did not test this).

Installation (for Linux/Unix)

NET-SNMP is easy to install. Just use the classic "./configure - make - make install" commands to execute configuration, compiling and installing of the software package. Anyhow, if you don't want to use Linux/Unix, there are also ports for Win32 or MacOS-X, but we did not try that. After installing the software you are in need of an additional MIB-file (Management Information Base), that defines the Viplax agent functions. This VIPLAX-MIB ca be obtained from the Viplax Web-Homepage (http://viplax-ip-address).

Before you are able to play with SNMP you have to copy this file (VIPLAX-MIB.txt) to the MIB directory onto your PC. If you have chosen a standard installation of NET-SNMP you have to use the directory /usr/local/share/snmp/mibs. This directory contains all known SNMP-MIBs from NET-SNMP.

SNMP at a glance

For the first test we do not need Viplax yet. Instead we will scan the structure of the previously installed Viplax-MIB. Please use the shell command:

```
snmptranslate -Tp -IR -m ALL inventronik
```

and you should see something like:

```
+--inventronik(22237)
  |
  +--viplaxSnmpMIB(1)
     |
     +--vsMIBComparators(1)
     | |
     | +-- -RW- Integer32 upperThresholdComp1(1)
     | |        Range: -100..100
     | +-- -RW- Integer32 lowerThresholdComp1(2)
     | |        Range: -100..100
     | +-- -RW- Integer32 upperThresholdComp2(3)
     | |        Range: -100..100
     | +-- -RW- Integer32 lowerThresholdComp2(4)
     |          Range: -100..100
     |
     +--vsMIBErrorHandling(2)
     | |
     | +-- -RW- EnumVal   enableErrorHandling(1)
     | |        Values: enabled(1), disabled(2)
     | +-- -RW- EnumVal   activateErrorStorage(2)
     | |        Values: enabled(1), disabled(2)
     | +-- -RW- Integer32 eraseErrorsPeriodically(3)
     | |        Range: 1..90
     | +-- -RW- Integer32 eraseErrorsOnce(4)
     |          Range: 1
     |
     +--vsMIBErrorCounters(3)
        |
        +-- -RW- Integer32 totalErrorsUpperComp1(1)
        +-- -RW- Integer32 totalErrorsLowerComp1(2)
        +-- -RW- Integer32 totalErrorsUpperComp2(3)
        +-- -RW- Integer32 totalErrorsLowerComp2(4)
```

The branches vsMIBComparators and vsMIBErrorHandling carry the basic Viplax parameters. We will show you how to read and write these parameters later. New, and exclusive to SNMP are 4 parameters in the branch vsMIBErrorCounters. These registers count for each threshold separately the oversteps. You can reset the registers anytime you want. After a new start of Viplax these registers have a zero value.

Read Viplax parameters

If you want to read back a Viplax parameter you will need the following command:

```
snmpget -m ALL -c viplax-ro -v 2c <ip-addr> VIPLAX-MIB::<Regname>.0
```

The read-only password is "viplax-ro", <ip-addr> is the IP address of the agent (Viplax) and <Regnamme> is the name of a leaf from Viplax MIB-structure, for example upperThresholdComp1. The trailing ".0" says that the value is a scalar type.

If you want to read all Viplax parameters at once, than you execute a snmpwalk command, here for example:

```
snmpwalk -m ALL -c viplax-ro -v 2c 192.168.1.52 inventronik
```

Change Viplax parameters

This is as easy as reading a Viplax parameter. The following command will write a new value into

the Viplax register.

```
snmpset -m ALL -c vplx9u1o1 -v 2c <ip-addr> VIPLAX-MIB::<Regname>.0 i <Value>
```

"vplx9u1o1" is the read-write password.

Unfortunately this password can't be changed; it is part of the ROM configuration. Later on we will support SNMP.V3 which will encrypt the password before it is sent over the network. After that we will add support for changeable password storage.

The command parameter "i" in the above command says that the value is an integer (Float values are not explicitly supported by SNMP). <Value> is the integer value of the Viplax parameter.

One important remark regarding eraseErrorsOnce: If you want to delete an error, you must write a zero value into the register. Reading a value different than zero means there has been an error triggered.

What's Next (To do):

We plan to extent the SNMP functionality and we will add trap support. Which traps we will covered has to be defined. Possibilities are:

- Authentication Trap: Wrong SNMP or HTTP password entered.
- Error Trap: As soon as an error has been triggered (probably in different classes).
- *Suggestions are welcome!*

Links:

- http://www.net-snmp.org – a lot about SNMP
- http://www.net-snmp.org/tutorial/tutorial-5/toolkit/mfd/ - MIB for Dummies
- http://www.enseirb.fr/~kadionik/embedded/snmp/english/net-snmp_english.html - SNMP for embedded Applications (very clear and easy to understand)

Changing the FPGA-Configware

Under normal circumstances it is not necessary to change the FPGA content of the Viplax receiver or sender. However, for exceptions to the rule, it might come in handy if there are minor changes.

The receiver contains the FPGA module 'Sphinx-C100-Rev.A' also produced by Inventronik GmbH. On our website, we provide a detailed documentation that explains the necessary steps to configure the FPGA. Programming must take place over the 'Active Serial' connector. The JTAG interface is not used.

The transmitter does not contain a 'Sphinx-C100-Rev.A' module, but the programming remains the same. The unused JTAG interface has been removed.

Changing the Microcontroller Firmware (MiniFlex only)

Again, under normal circumstances there is no need to change the firmware. In the interests of software flexibility there is a possibility to make adjustments to the firmware to meet special requirements in industrial and scientific applications. Please contact us with your specifications.

The USB version of the Viplax receiver uses the 'MiniFlex-USB' developed by Inventronik GmbH. The documentation in the download area of our website explains how to program the controller.

Software Support

Inventronik GmbH offers development services to extend or expand the functionality of Viplax. Please contact us if you have further questions.

Appendix

Technical Data

Transmitter_V3_RevA, Receiver_V3_RevA:

Input Amplifier:
Input voltage range: ± 0.25V; ± 1.0V; ± 2.5V; ± 4.0V; ± 10.0V.
Voltage Gain: 32dB; 20dB; 12dB; 8dB; 0dB (adjustable).

Anti-Aliasing-Filter:
Bessel Low Pass Filter 4th Order:
3dB Frequency: 2.5MHz
Voltage Drop near the 3dB Frequency: 20dB/Octave.
Remark: The theoretical voltage drop of 24dB is not reached due to the not ideal but nevertheless accurate behavior of the installed operational amplifiers.

A/D-Wandler:

Resolution:	14 bit.
Samplingrate:	10Mbps.
Signal to Noise Ratio:	>75dB.
Integral Linearity Error:	± 2.5 LSB.
Differential Nonlinearity:	± 1 LSB.

Further information: see the Analog Devices AD9240 data sheet.

Digitale Signal Processing:

Signal Latency:	< 2.5µs
System Bandwidth:	2.5MHz
Window Comparators:	bipolar, adjustable.
System Status Bits:	A/D-Overflow; Battery Load Condition, System Error, Comparator Thresholds.
Digital Inputs:	5 Pin (Transmitter), 7 Pin (Receiver).
Digital Outputs:	5 Pin (Transmitter), 7 Pin (Receiver).
Output voltage levels:	5V at the VG type connector, 3.3V at the pin headers.
Current:	10mA.
Input voltage levels:	TTL tolerant.
Visualisation:	All relevant System Status Bits via LEDs.

Fiber Optics:

Maximum Bit Stream Frequency:	200Mbaud.
Optical Wave Lenght	1300nm.
Fiber Type:	50µm oder 62.5µm core, multimode.
Connector:	ST Type.
Maximum Length:	1000m. (the maximum achievable length is dependant on the quality and condition of the fiber optic cable.)
User definable Gains:	1.176 (Stellung SJ3: 2-3; Stellung SJ4: x1.176; U_{inmax} =2.126V) 0.294 (Stellung SJ3: 1-2; Stellung SJ4: x1.176; U_{inmax} =8.503V)

D/A converter:

Resolution:	14 bit.
Sampling Rate:	125Mbps.
Spurious Free Dynamic Range:	>75dB.
Integral Linearity Error:	± 4.5 LSB.
Differential Nonlinearity:	± 1.5 LSB (typ).

Further information: see the Analog Devices AD9764 data sheet.

Output Amplifier (Twin Amplifier):

Output Voltage Range:	± 10.0V (full conduction).
Output Impedance:	50 Ohm, 75 Ohm.

Voltage Supply:

Transmitter:	12 VAC / 1.2A.
Receiver:	15VAC / 0.25A; 15 VAC / 0.25A; 9VAC / 1.4A.

As mentioned above: we do not recommend the use of switched mode power supplies!

Connector Pinouts

Signal	*Connector Pin*	*Signal*	*Connector Pin*
GND	PIN1	GND	PIN2
RA5 (not used)	PIN3	RA0 (not used)	PIN4
RA4 (not used)	PIN5	RA1 (not used)	PIN6
RA3 (not used)	PIN7	RA2 (not used)	PIN8
+5V	PIN9	+5V	PIN10

Table 11: Connector SV1; Receiver.

Signal	*Connector Pin*	*Signal*	*Connector Pin*
GND	PIN1	GND	PIN2
RC5 (not used)	PIN3	RC0 (not used)	PIN4
STDP (not used)	PIN5	RC1 (not used)	PIN6
not connected	PIN7	RC2 (not used)	PIN8
+5V	PIN9	+5V	PIN10

Table 12: Connector SV2; Receiver.

Connector Pin	*Signal*	*Connector Pin*	*Signal*
X5-A1	*DA_D13*	X5-C1	15V AC I
X5-A2	DA_D12	X5-C2	15V AC I
X5-A3	DA_D11	X5-C3	GND
X5-A4	DA_D10	X5-C4	GND
X5-A5	DA_D9	X5-C5	GND
X5-A6	DA_D8	X5-C6	GND
X5-A7	DA_D7	X5-C7	GND
X5-A8	DA_D6	X5-C8	GND
X5-A9	DA_D5	X5-C9	GND
X5-A10	DA_D4	X5-C10	GND
X5-A11	DA_D3	X5-C11	GND
X5-A12	DA_D2	X5-C12	GND
X5-A13	DA_D1	X5-C13	GND
X5-A14	DA_D0	X5-C14	GND
X5-A15	DA_D_VALID (Memory)	X5-C15	GND
X5-A16	*LINK_FLT (Memory)*	X5-C16	9V AC
X5-A17	COMP_1L (Memory)	X5-C17	9V AC
X5-A18	COMP_1H (Memory)	X5-C18	GND
X5-A19	COMP_2L (Memory)	X5-C19	GND
X5-A20	COMP_2H (Memory)	X5-C20	GND

Connector Pin	*Signal*	*Connector Pin*	*Signal*
X5-A21	COMP_FAULT (Memory)	X5-C21	GND
X5-A22	LOW_BAT (Memory)	X5-C22	GND
X5-A23	AD_FLT	X5-C23	GND
X5-A24	D_OUT6 (RESETn)	X5-C24	GND
X5-A25	*D_IN6 (clear fault memory)*	X5-C25	GND
X5-A26	*D_IN5 (not used)*	X5-C26	GND
X5-A27	*D_IN4 (not used)*	X5-C27	GND
X5-A28	*D_IN3 (not used)*	X5-C28	GND
X5-A29	*D_IN2 (not used)*	X5-C29	GND
X5-A30	*D_IN1 (not used)*	X5-C30	GND
X5-A31	*FLAG1 (not used)*	X5-C31	15V AC II
X5-A32	*FLAG2 (not used)*	X5-C32	15V AC II

Table 13: Connector X5; Receiver.

Signal	*Connector Pin*	*Signal*	*Connector Pin*
+5V	PIN1	+5V	PIN2
D_OUT6 (RESETn)	PIN3	D_OUT5 (LINK_RDY)	PIN4
D_OUT4 (AD_FLT)	PIN5	D_OUT3 (COMP_FLT)	PIN6
D_OUT2 (LOW_BAT)	PIN7	D_OUT1 (GB_BIT7)	PIN8
GND	PIN9	GND	PIN10

Table 14: Connector X6; Receiver.

Signal	*Connector Pin*	*Signal*	*Connector Pin*
+5V	PIN1	+5V	PIN2
D_IN6 (not used)	PIN3	D_IN5 (not used)	PIN4
D_IN4 (not used)	PIN5	D_IN3 (not used)	PIN6
D_IN2 (not used)	PIN7	D_IN1 (not used)	PIN8
GND	PIN9	GND	PIN10

Table 15: Connector X7; Receiver.

Signal	*Connector Pin*	*Signal*	*Connector Pin*
COMP1_L	PIN1	COMP1_H	PIN2
COMP2_L	PIN3	COMP2_H	PIN4
LINK_FLT	PIN5	LOW_BAT	PIN6
AD_FLT	PIN7	COMP_FAULT	PIN8
GND	PIN9	GND	PIN10

Table 16: Connector X10; Receiver.

Connector Pin	*Signal*	*Connector Pin*	*Signal*
X11-PIN1	*+5V*	X11-PIN11	DA_D5
X11-PIN2	*+5V*	X11-PIN12	DA_D4
X11-PIN3	DA_D13	X11-PIN13	DA_D3
X11-PIN4	DA_D12	X11-PIN14	DA_D2
X11-PIN5	DA_D11	X11-PIN15	DA_D1
X11-PIN6	DA_D10	X11-PIN16	DA_D0
X11-PIN7	DA_D9	X11-PIN17	DA_D_VALID
X11-PIN8	DA_D8	X11-PIN18	AD_FLT
X11-PIN9	DA_D7	X11-PIN19	*GND*
X11-PIN10	DA_D6	X11-PIN20	*GND*

Table 17: Connector X11; Receiver.

Signal	*Connector Pin*	*Signal*	*Connector Pin*
I/O (not used)	PIN1	GND	PIN2
I/O (not used)	PIN3	I/O (not used)	PIN4
I/O (not used)	PIN5	I/O (not used)	PIN6
I/O (not used)	PIN7	I/O (not used)	PIN8
I/O (not used)	PIN9	3,3V	PIN10

Table 18: Connector SV2; Transmitter.

Simulation Plots of the Anti-Aliasing Filter in the transmitter.

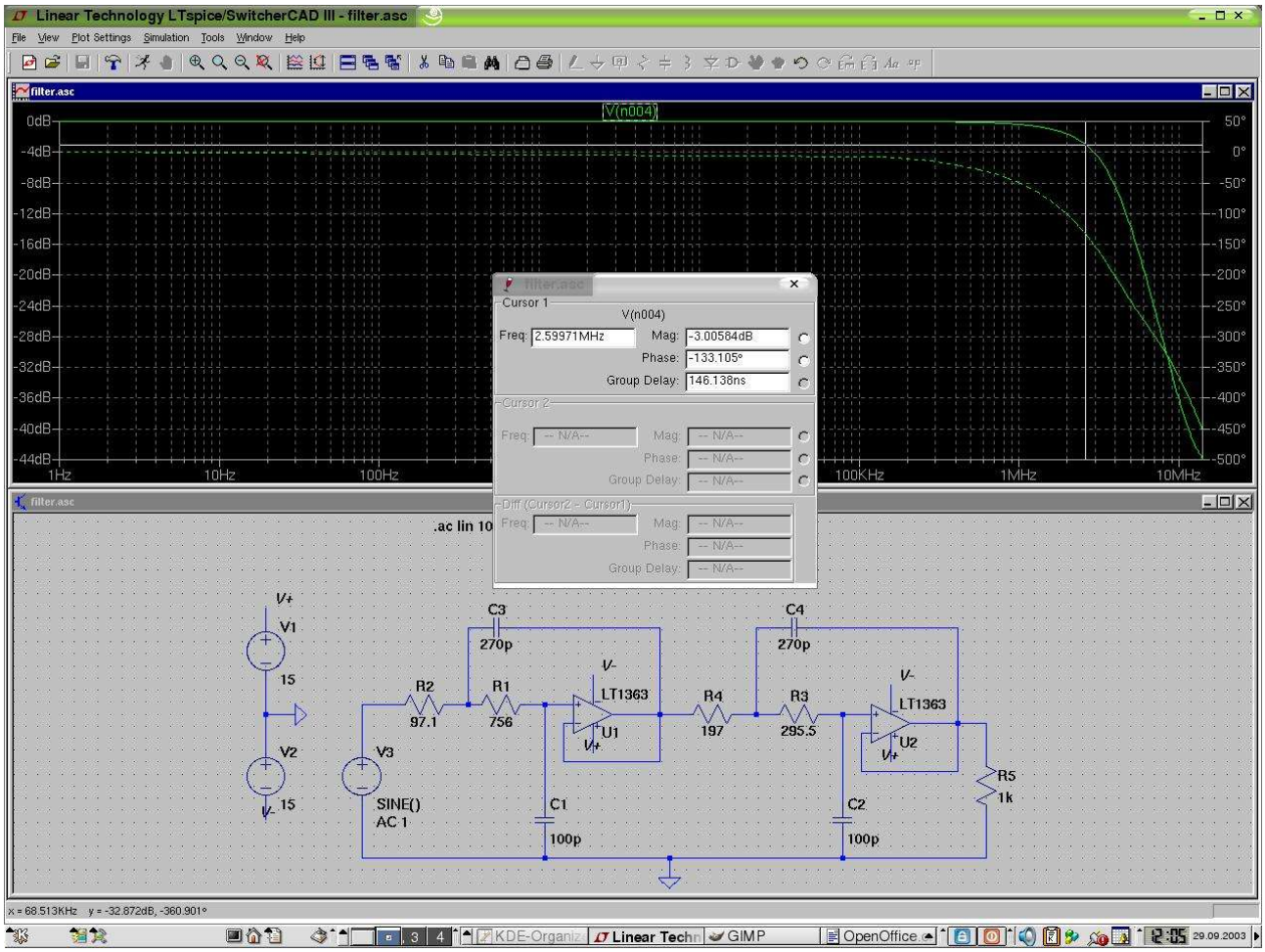


Figure 23: Simulation screenshot of the Anti-Aliasing filters. The upper curve prints the simulation of the absolute value, the lower curve is the phase. The -3dB point has a value of ca. 2.5MHz. The signal bandwidth is therefore about 2 MHz. The dialog window contains data of the -3dB point. The schematic shows the used Bessel Filter.

Test Procedure for Transmitter and Receiver

To guarantee a high product quality for every Viplax transmitter/receiver we adjusted them pairwise. The test procedure is written down in a test protocol and is done in three steps: the transmitter-, the receiver- and the system-test (transmitter and receiver are operating together).

Transmitter Functional Tests:

- Basic functions (JTAG programming, voltage tests)
- Comparator functionality
- Error system
- Visualisation
- Amplifier functionality

Receiver Functional Tests:

- Basic functions (JTAG programming, voltage tests)
- Comparator functionality
- Error system
- Visualisation
- Test of the output amplifier
- Test of the USB/Ethernet configuration interface
- Test of the RS-232 interface (if available)
- Digital inputs and digital outputs.

During the tests the absolute accuracy of the gain is adjusted, and the components are operated over 48 hours (burn-in test).

Finally the transmitter and the receiver are marked pairwise and operated together in a last system test where the data of the test protocol are evaluated.

Test Protocol of the Viplax System

The Viplax Transmitter and Viplax Receiver are marked pairwise. The measured parameters are valid for pairs. The measurement protocol as shown here contains no values because these protocols are completed individually and shipped with every Viplax pair.

Inventronik GmbH.
Kompetente Lösungen für Ihre Ideen

Finkenstraße 48
70199 Stuttgart

Inventronik Stuttgart - Finkenstr. 48 - D-70199 Stuttgart

Tel: +49 - (0)711 - 60 19 637
FAX: +49 - (0)711 - 60 19 638
Mail: post@inventronik.de
Internet: www.inventronik.de

Prüfprotokoll Viplax Rev.A RT/17

Grenzfrequenz und Signalverzögerung:

3dB Genzfrequenz (1):
f =

Signalverzögerung zwischen Eingang und Ausgang gemessen an einem Rechtecksignal (bei 50% Amplitude und 1kHz Frequenz):
td =

Absolutgenauigkeiten des Viplax Receiver/Transmitter-Paars:

Jumper SJ3:	*1-2*	*2-3*	*1-2*	*2-3*	*2-3*	*1-2*	*2-3*	*1-2*	*2-3*
Jumper SJ4:	x1	x1	x2.5	x2.5	x10	x2..10	x2..10	x1.176	x1.176
U_{inmax}	±10V	±2.5V	±4V	±1V	±0.25V	±5..1V	±1.25..0.25V	±8.503V	±2.126V
U_{in} / U_{BNC}	0.5	2.0	1.25	5.0	20.0	1...5	4...20	0.588	2.358
U_{in} / U_{SMB}	1.0	4.0	2.5	10.0	40.0	2...10	8...80	1.176	4.717
Eingangs-spannung	5V	1.25V	2V	0.5V	0.125V	2.5V	1V	4V	1V
Ausgangs-spannung									
relativer Fehler									

Funktionschecks:

Fehlerauslösung:

Link-Fault: ok AD-Fault: ok Comp-Fault: ok
Low-Batterie: ok

Fehlerverriegelung:

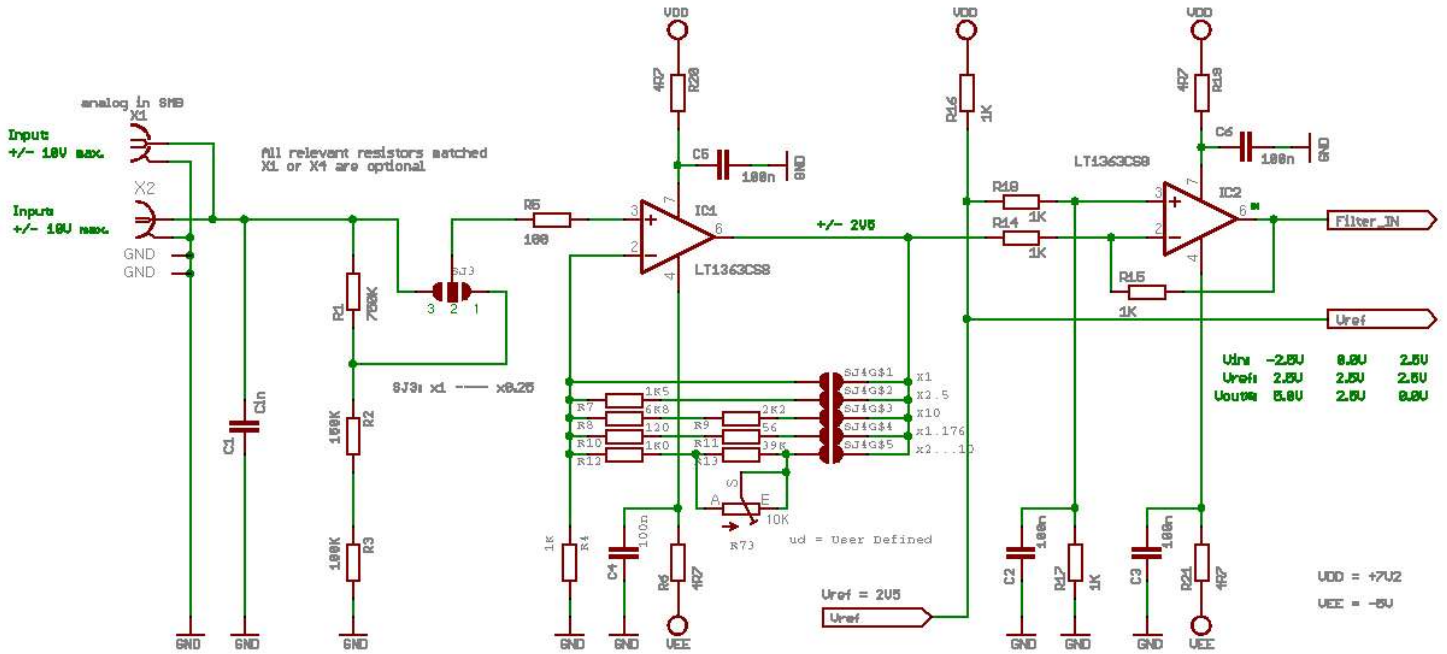
First Fault Memory: ok Fehlersystem-Abschaltung: ok

Messungen ausgeführt, abgenommen von:

Datum: _____ Unterschrift: _____

(1) Die Viplax-Systeme können prinzipiell Frequenzen bis 2.5MHz verarbeiten. Bei Ausnutzung der vollen Bandbreite von 2.5MHz resultiert im Frequenzbereich um 1.5MHz eine Amplitudenüberhöhung (< 3dB), die sich bei Verarbeitung von Rechtecksignalen in den Flanken bemerkbar macht. Im Sinne einer optimalen Signalverarbeitung im interessierenden Frequenzbereich sind die Viplax-Empfänger auf eine 3dB-Grenzfrequenz zwischen 2.0MHz und 2.2MHz eingestellt.

Printed circuit diagram of the transmitter



Voltage ranges:

SJ3:	1-2	2-3	1-2	2-3	1-2	2-3	1-2	2-3	1-2	2-3
SJ4:	x1	x1	x2.5	x2.5	x10	x10	x1.176	x1.176	x2..10	x2..10
U-in_max:	+/-10V	+/-2.5V	+/-4V	+/-1V	+/-1V	+/-0.25V	+/-8.503V	+/-2.126V	--	--

Inventronik GmbH, 2004

Eingangsverstärker

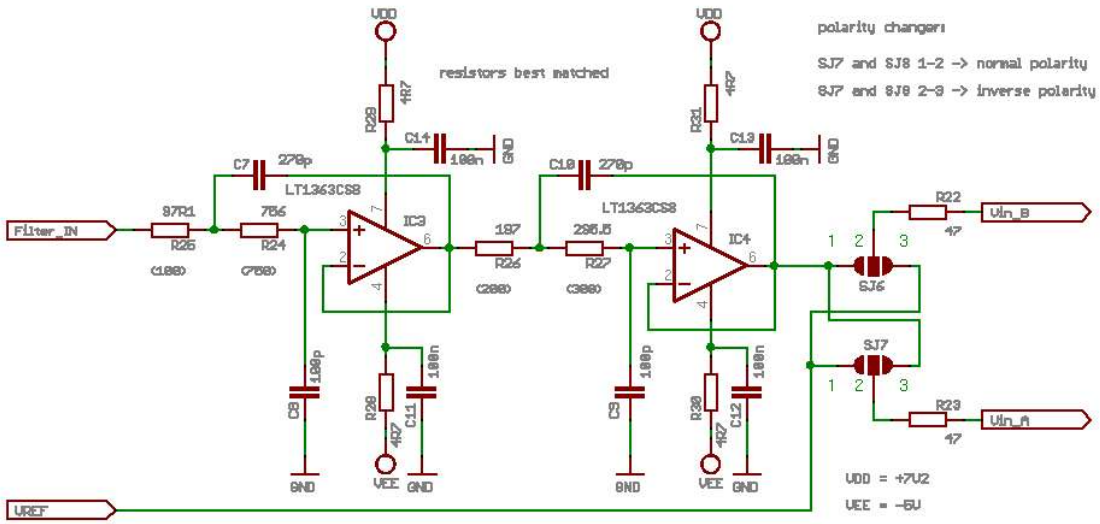
TITLE: transmitter_v3_revA

Document Number: Viplax_ED_02-2004
WF, JC, Änderungen vorbehalten

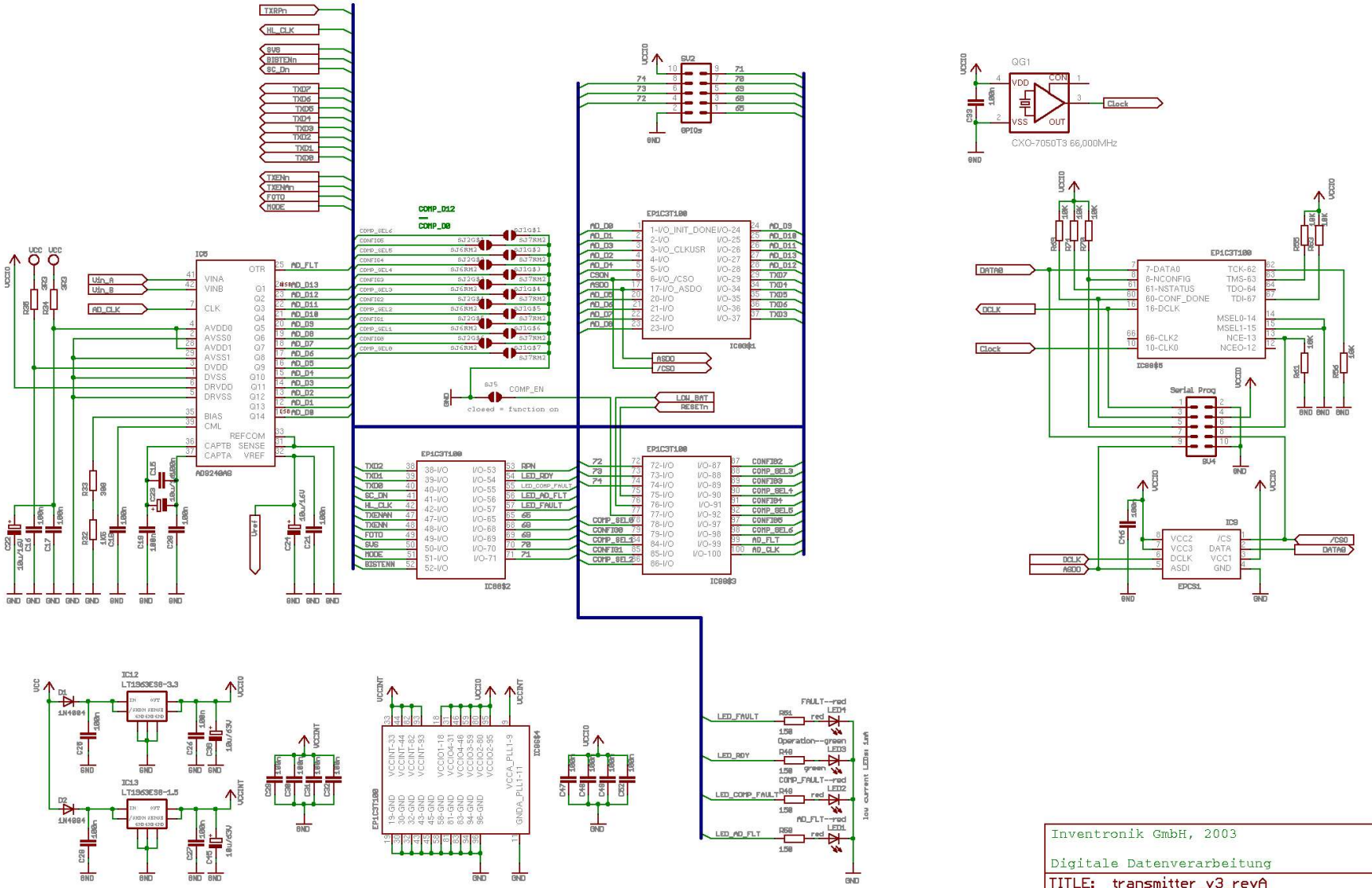
REV: 1.3

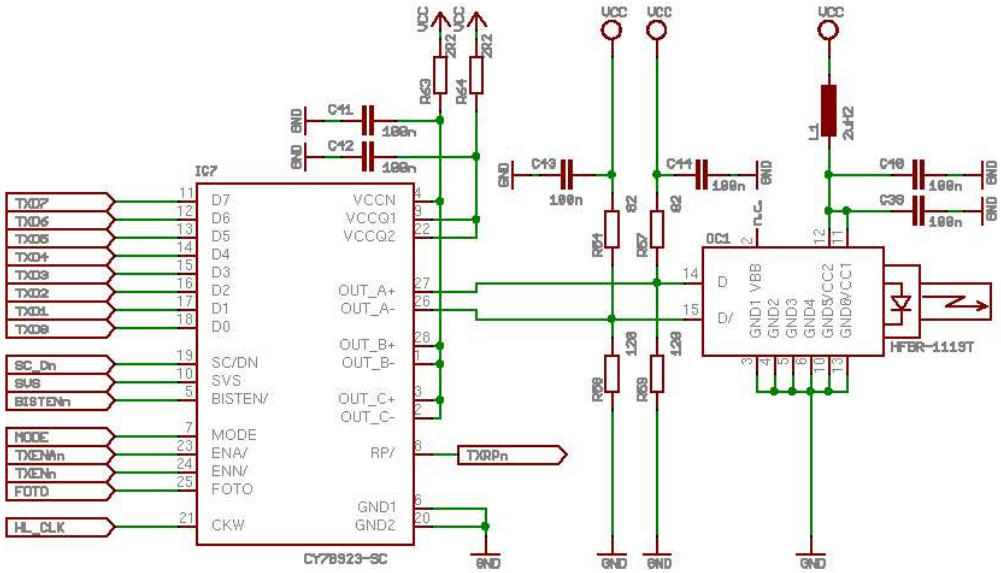
Date: 5/19/2004 10:30:11

Sheet: 1/5

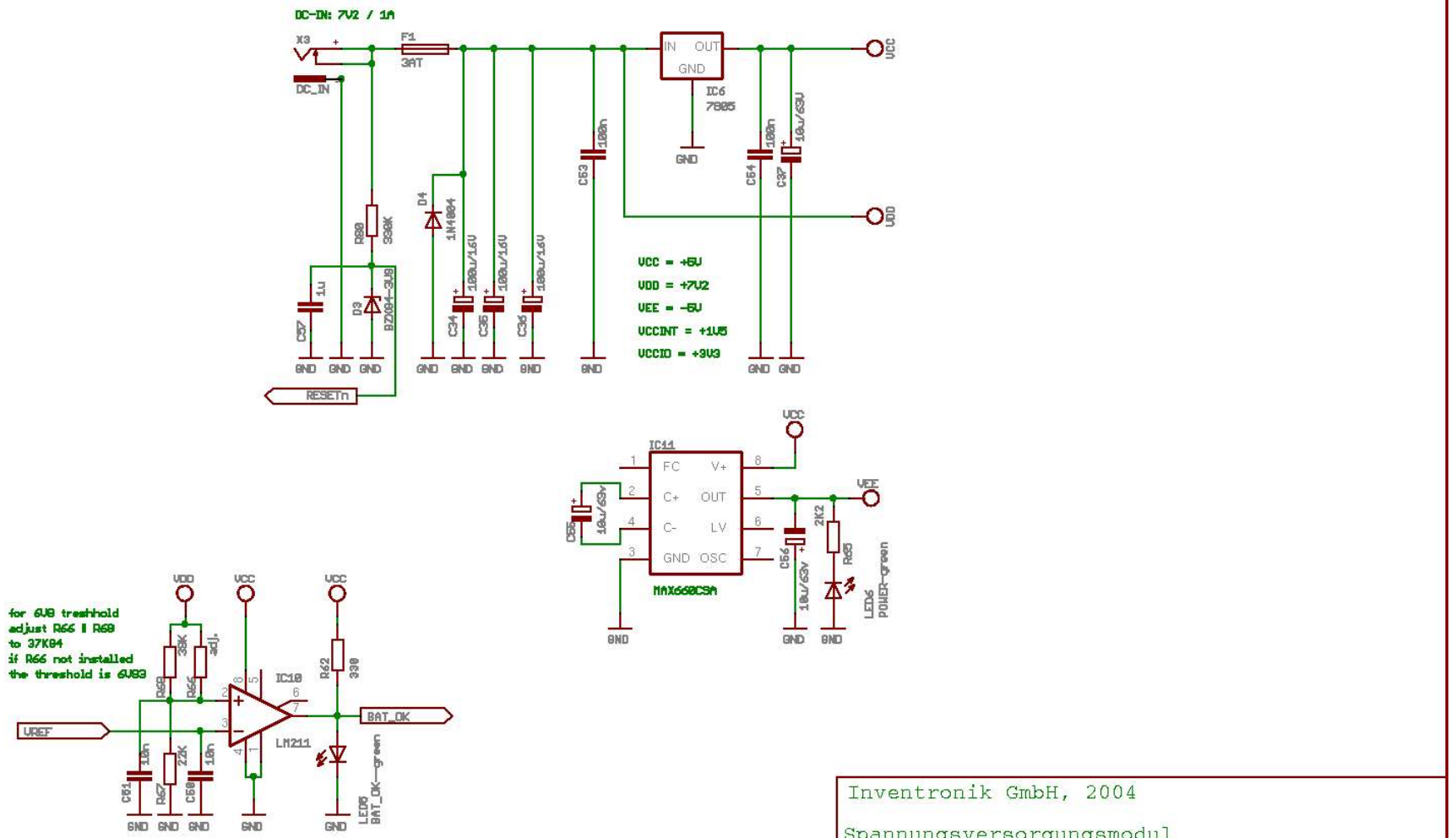


Inventronik GmbH, 2004		
Anti Aliasing Filter; BW = 2,5 MHz		
TITLE: transmitter_v3_revA		
Document Number: Viplax_ED_02-2004 WF, JC, Änderungen vorbehalten		REV: 1.3
Date: 5/19/2004 10:30:11	Sheet: 2/5	


TXRPn
HL_CLK
SYS
BISTENn
SC_DN
TXD7
TXD6
TXD5
TXD4
TXD3
TXD2
TXD1
TXD0
TXENn
TXENMn
FOTO
MODE
COMP_D12
COMP_D0
IC5
AD9240AS
Vin_A
Vin_B
AD_CLK
AD_FLT
AD_D13
AD_D12
AD_D11
AD_D10
AD_D9
AD_D8
AD_D7
AD_D6
AD_D5
AD_D4
AD_D3
AD_D2
AD_D1
AD_D0
SJ5
COMP_EN
closed = function on
LOW_BAT
RESETn
ASDO
/CSO
SV2
GPIOs
EP1C3T100
IC8@1
IC8@2
IC8@3
IC8@4
IC8@5
IC8@6
QG1
CXO-7050T3 66,000MHz
Clock
DATA0
DCLK
Serial Prog
SV4
IC9
EPCS1
IC12
LT1963ES8-3.3
IC13
LT1963ES8-1.5
D1
D2
1N4004
LED_FAULT
LED_RDY
LED_COMP_FAULT
LED_AD_FLT
FAULT--red
LED4
Operation--green
LED3
COMP_FAULT--red
LED2
AD_FLT--red
LED1
low current LEDs: 1mA
Inventronik GmbH, 2003
Digitale Datenverarbeitung
TITLE: transmitter_v3_revA
Document Number: Viplax_ED_06-2003
WF, JC, Änderungen vorbehalten
REV: 1.3
Date: 5/19/2004 10:30:11
Sheet: 3/5

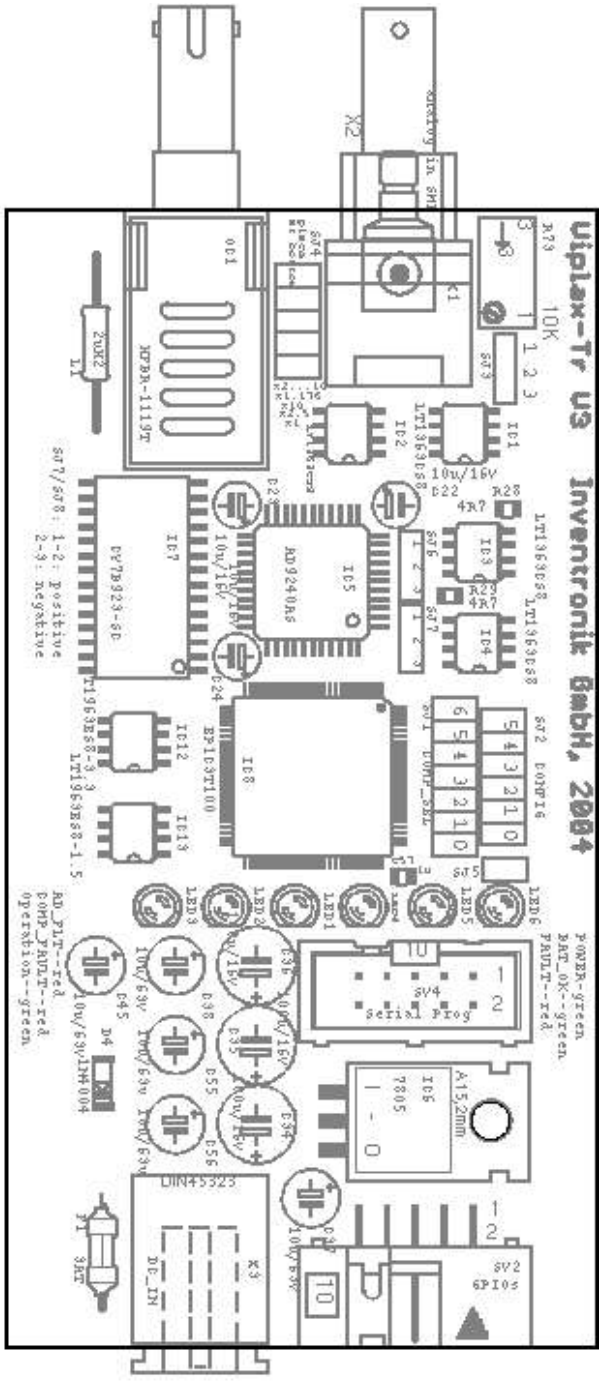


Inventronik GmbH, 2004		
Bitstream Wandler		
TITLE: transmitter_v3_revA		
Document Number: Viplax_ED_02-2004 WF, JC, Änderungen vorbehalten		REV: 1.3
Date: 5/19/2004 10:30:11	Sheet: 4/5	

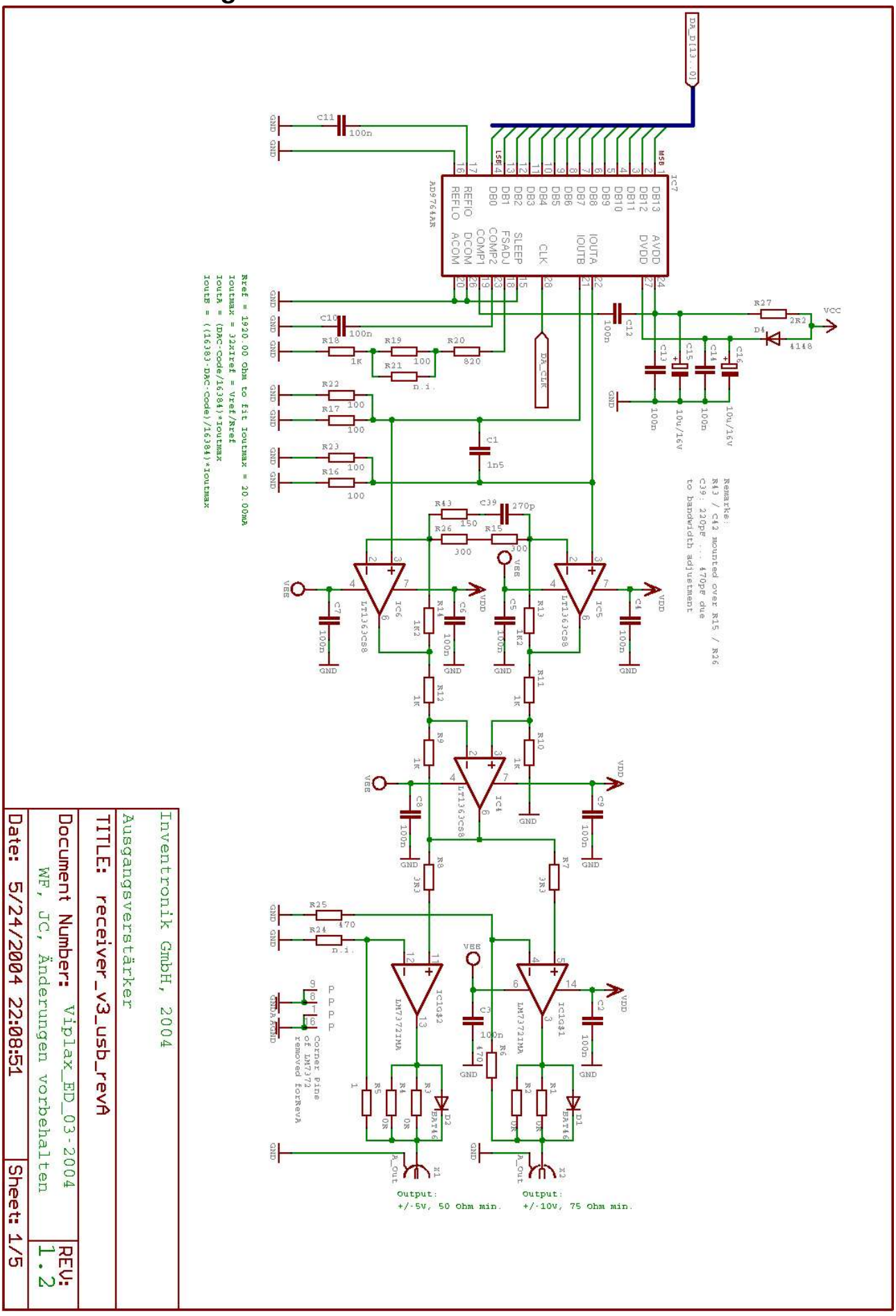


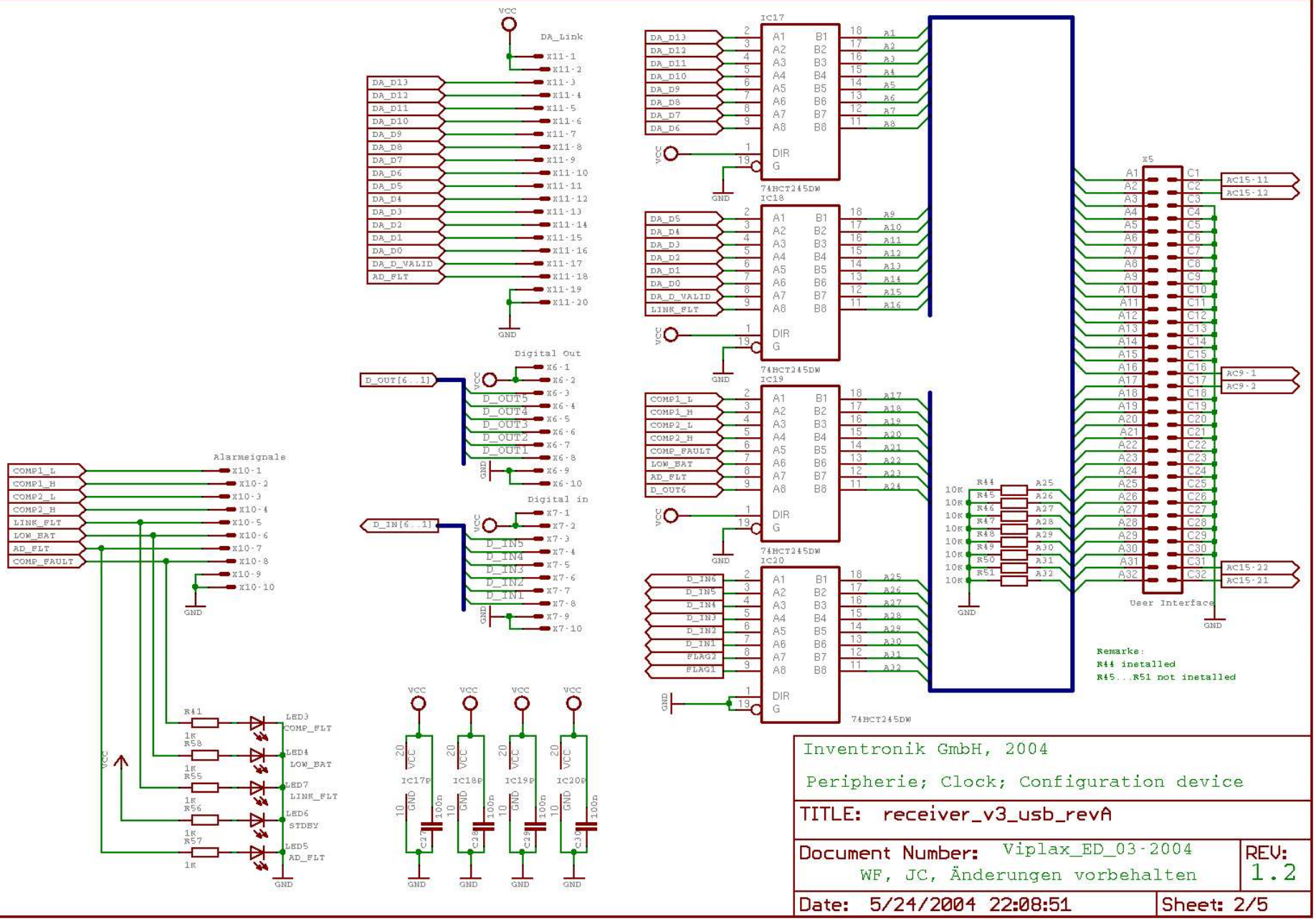
Inventronik GmbH, 2004		
Spannungsversorgungsmodul		
TITLE: transmitter_v3_revA		
Document Number: Viplax_ED_02-2004 WF, JC, Änderungen vorbehalten		REV: 1.3
Date: 5/19/2004 10:30:11	Sheet: 5/5	

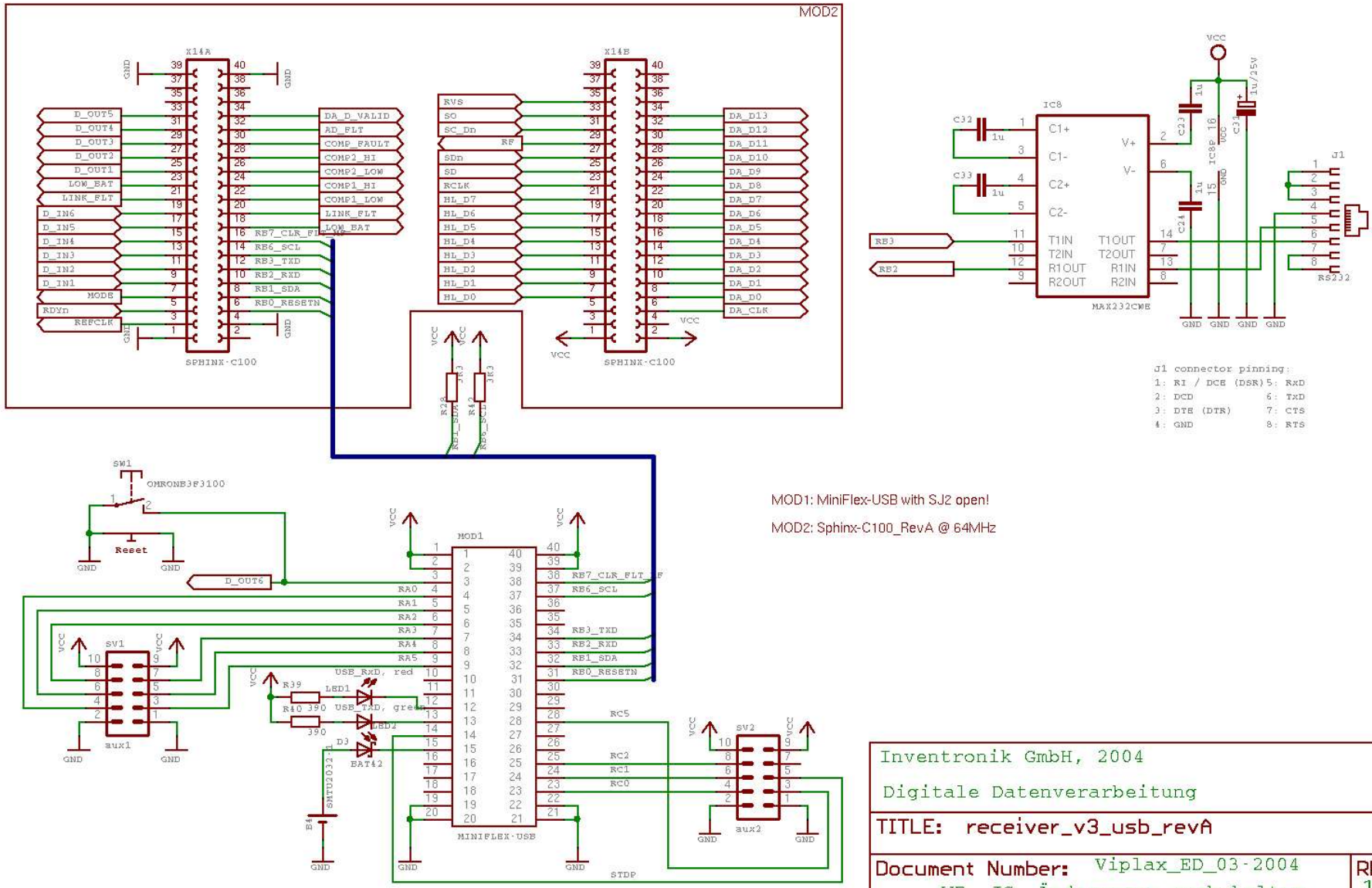
Layout of the electronic components of the transmitter

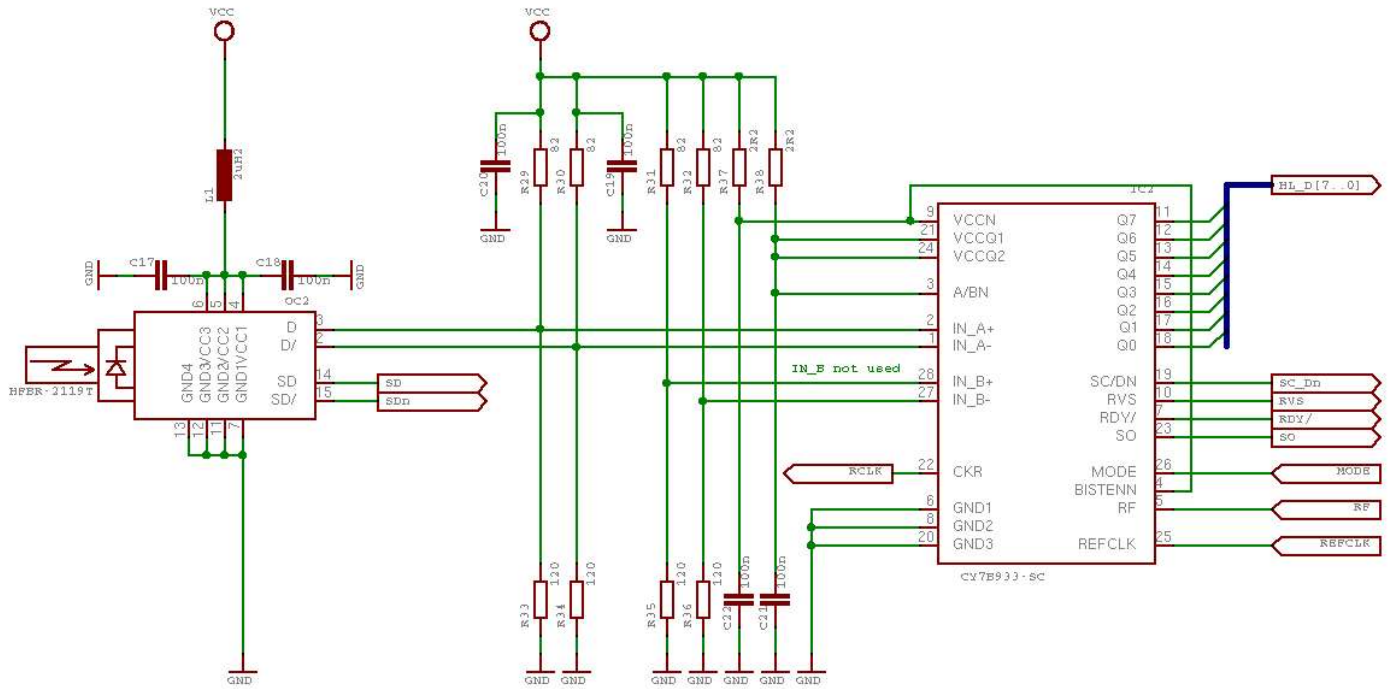


Printed circuit diagram of the Receiver

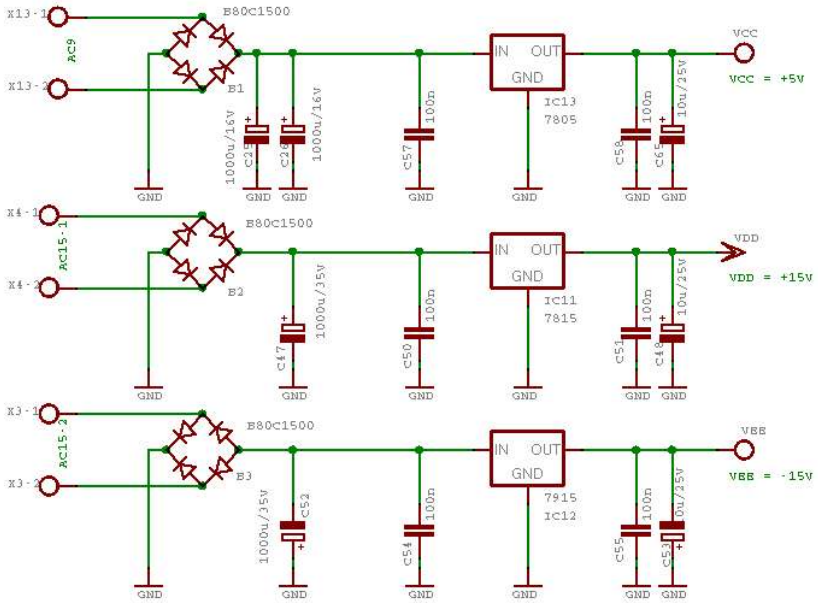



DA_Link
Digital Out
Digital in
Alarmeignale
74HCT245DW
Ueer Interface
Remarke:
R44 installed
R45...R51 not installed
Inventronik GmbH, 2004
Peripherie; Clock; Configuration device
TITLE: receiver_v3_usb_revA
Document Number: Viplax_ED_03-2004
WF, JC, Änderungen vorbehalten
REV: 1.2
Date: 5/24/2004 22:08:51
Sheet: 2/5


MOD2
X14A
X14B
SPHINX-C100
SPHINX-C100
D_OUT5
D_OUT4
D_OUT3
D_OUT2
D_OUT1
LOW_BAT
LINK_FLT
D_IN6
D_IN5
D_IN4
D_IN3
D_IN2
D_IN1
MODE
RDYn
REFCLK
DA_D_VALID
AD_FLT
COMP_FAULT
COMP2_HI
COMP2_LOW
COMP1_HI
COMP1_LOW
LINK_FLT
LOW_BAT
RB7_CLR_FLT
RB6_SCL
RB3_TXD
RB2_RXD
RB1_SDA
RB0_RESETN
RVS
SO
SC_Dn
RF
SDn
SD
RCLK
HL_D7
HL_D6
HL_D5
HL_D4
HL_D3
HL_D2
HL_D1
HL_D0
DA_D13
DA_D12
DA_D11
DA_D10
DA_D9
DA_D8
DA_D7
DA_D6
DA_D5
DA_D4
DA_D3
DA_D2
DA_D1
DA_D0
DA_CLK
VCC
GND
R39
R42
3K3
RB1_SDA
RB6_SCL
IC8
C1+
C1-
C2+
C2-
V+
V-
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
MAX232CWE
C32
C33
C23
C24
C31
1u
1u/25V
IC8e 16
J1
RS232
RB3
RB2
J1 connector pinning:
1: RI / DCE (DSR)
2: DCD
3: DTE (DTR)
4: GND
5: RxD
6: TxD
7: CTS
8: RTS
SW1
OMRONB3F3100
Reset
D_OUT6
MOD1
MINIFLEX-USB
RA0
RA1
RA2
RA3
RA4
RA5
RB7_CLR_FLT
RB6_SCL
RB3_TXD
RB2_RXD
RB1_SDA
RB0_RESETN
RC5
RC2
RC1
RC0
STDP
SV1
aux1
SV2
aux2
USB_RxD, red
USB_TxD, green
LED1
LED2
R39
R40 390
390
D3
BAT42
E4
SMTU2032-H
MOD1: MiniFlex-USB with SJ2 open!
MOD2: Sphinx-C100_RevA @ 64MHz
Inventronik GmbH, 2004
Digitale Datenverarbeitung
TITLE: receiver_v3_usb_revA
Document Number: Viplax_ED_03-2004
WF, JC, Änderungen vorbehalten
REV: 1.2
Date: 5/24/2004 22:08:51
Sheet: 3/5

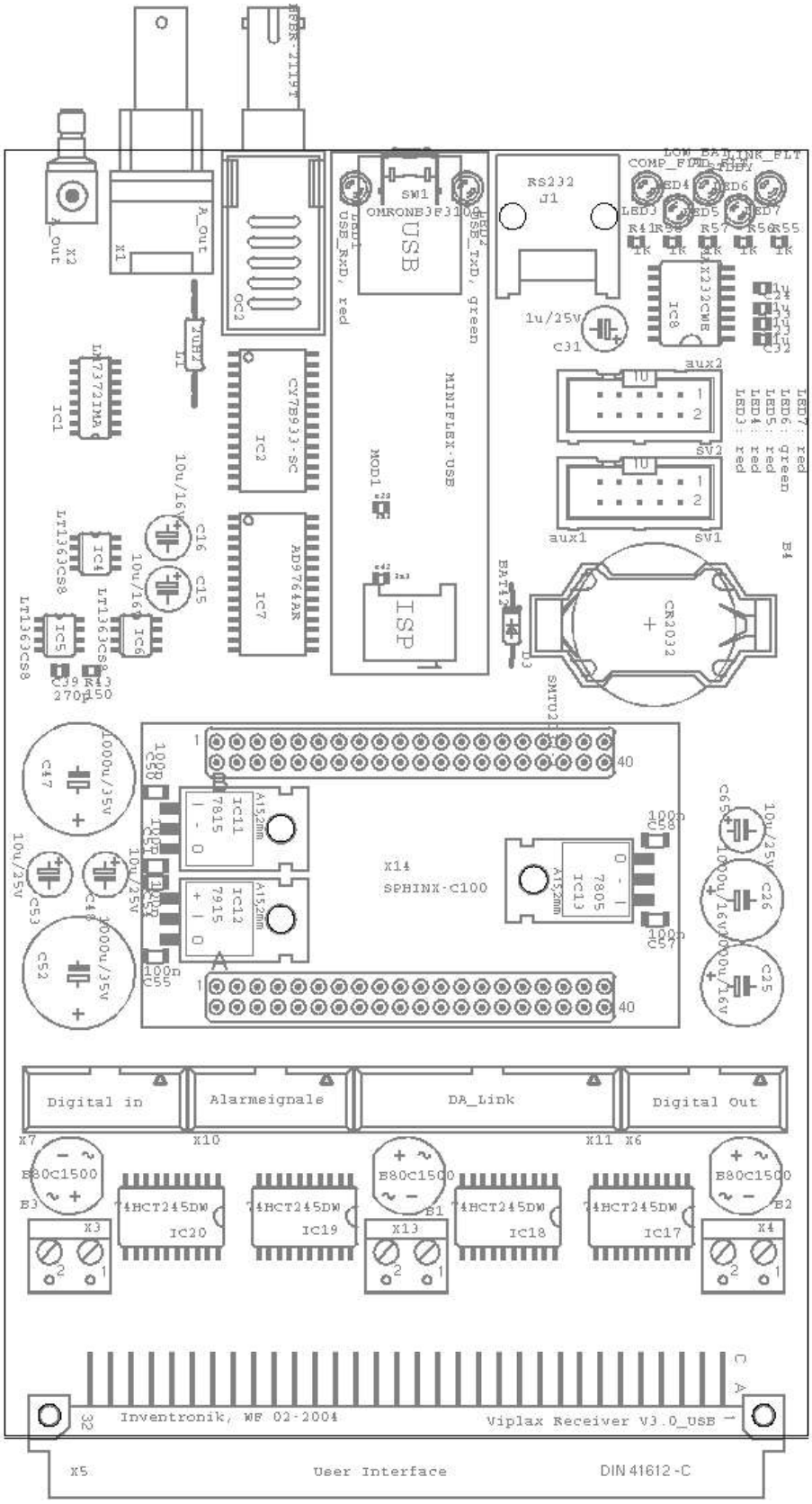


Inventronik GmbH, 2004		
Opto-Empfänger und Bitstream-Wandler		
TITLE: receiver_v3_usb_revA		
Document Number: Viplax_ED_03-2004 WF, JC, Änderungen vorbehalten		REV: 1.2
Date: 5/24/2004 22:08:51	Sheet: 4/5	



Inventronik GmbH, 2004 Netzteil		
TITLE: receiver_v3_usb_revA		
Document Number: Viplax_ED_03-2004 WF, JC, Änderungen vorbehalten		REV: 1.2
Date: 5/24/2004 22:08:51	Sheet: 5/5	

Layout of the electronic components of the receiver



Accessories

Receiver Power Supply

The Viplax receiver requires three supply voltages. 9V-AC and two times 15V-AC. Inventronik GmbH delivers a power supply which is designed for this purpose (Figure 25). The power supply delivers 9V with a current of 2,78A and 15V with each 0,83A. The power is sufficient to operate two Viplax receivers with one power supply. The supply is designed for mains of 230V. Other versions are available on request. The form factor is provided for installation in 19” subracks. The sizes are 3U and 14HU.

Figure 25:

Figure 24:

Figure 24 shows the rear panel of the power supply. The connector is a DIN41612 version H15. The pinout is shown in the following table:

Signal	*Connector Pin*	*Signal*	*Connector Pin*
9V-AC_1	Z4 and D6	N	Z28
9V-AC_2	Z8 and D10	L	D30
15V-AC-I_1	Z16	PE	Z32
15V-AC-I_2	D18		
15V-AC-II_1	Z20	no used	Z12, Z24, D14
15V-AC-II_2	D22	no Pin	D26

Table 19: Pinout of the power supply connector.

The 9V supply voltage has two pins for each pole. The first 15V voltage source is connected to Z16 and D18 and the second one to Z20 and D22.

The mains (230V-AC) are connected to the pins Z28 (Null), D30 (Phase) and Z32 (Protection Earth). Due to safety reasons, the pin D26 is removed.
Attention: the pins Z28 and D30 may not be interchanged!

On the front panel of the power supply are four LEDs. Three (green) indicate the correct operation of the three voltages ('15V-AC-II', '15V-AC-I' und '9V-AC') and the fourth one (red) is used for the

supervision of the fuse. In normal operation the green LEDs are 'on' and the red one is 'off'. If the fuse is blown, the red LED is 'on'.

Hint: If the power supplies are connected to a weak load, the red LED may shine a little bit even if the fuse is ok. This is due to leakage current of the fuse fault circuit and does not indicate a malfunction of the power supply.

A defective fuse must be exchanged with the correct value of 2AT. The fuse form factor is (4x20mm), glass tube type.

Backplane Basic and Basic-Bi

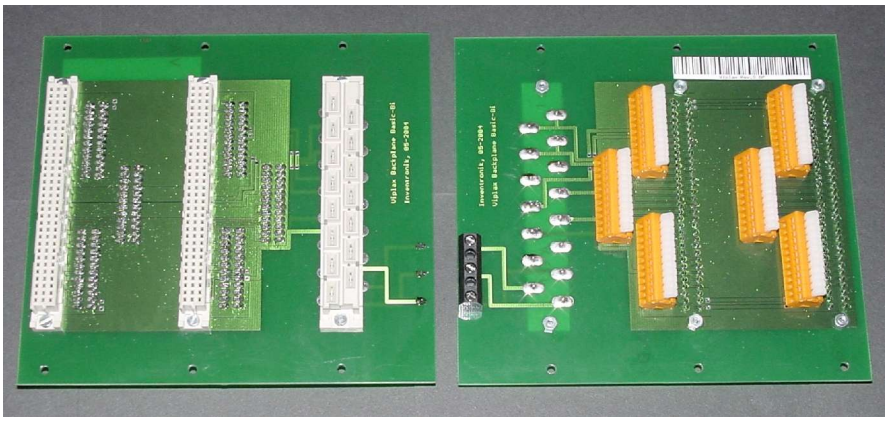


Figure 26: Front- und Rear-view of the Backplane Basic-Bi

Wiring one or two Viplax receivers with one receiver power supply, Inventronik GmbH offers two different backplanes. They are designed for the use in 19” subracks. The version ***Backplane Basic*** connects one Viplax receiver with a power supply and the ***Backplane Basic-Bi*** is built to assemble two receivers to one power supply.

The backplanes are mounted directly to 19” subracks with small auxiliary parts (distances of 3mm) but without “Z-Schienen”. This construction supports isolation of the mains potential from the normally to earth ground connected subrack. To ease the installation, the backplane is marked on the front side with *TOP*. Mounted, the Viplax receivers are located to the left of the power supply.

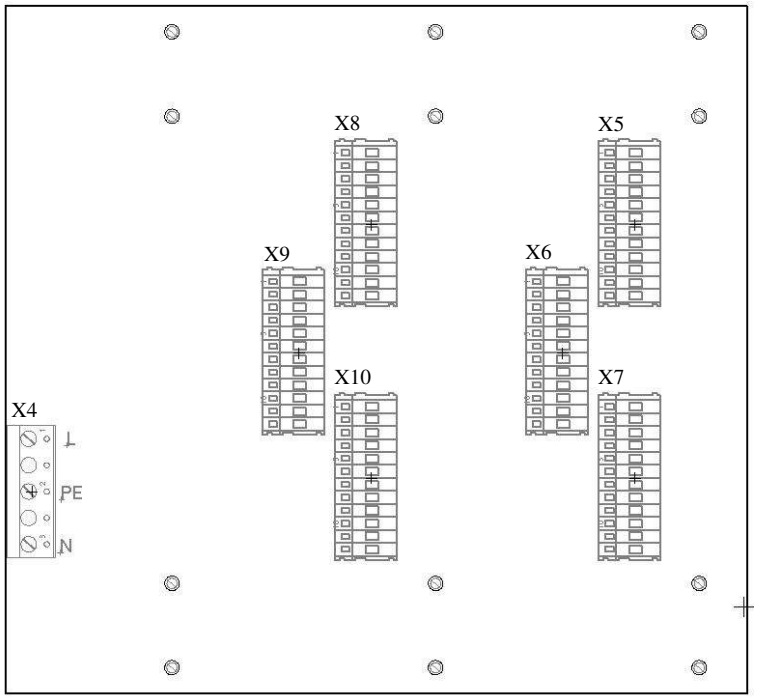


Figure 27: Backplane Basic-Bi rear view

On the rear side there are four terminals for the Backplane Basic and 7 terminals for the Basic-Bi. The small one (X4) is wired to the mains. The pinout is shown in Figure 27.

Important: The pin-out of the mains connector has to be done as follows:

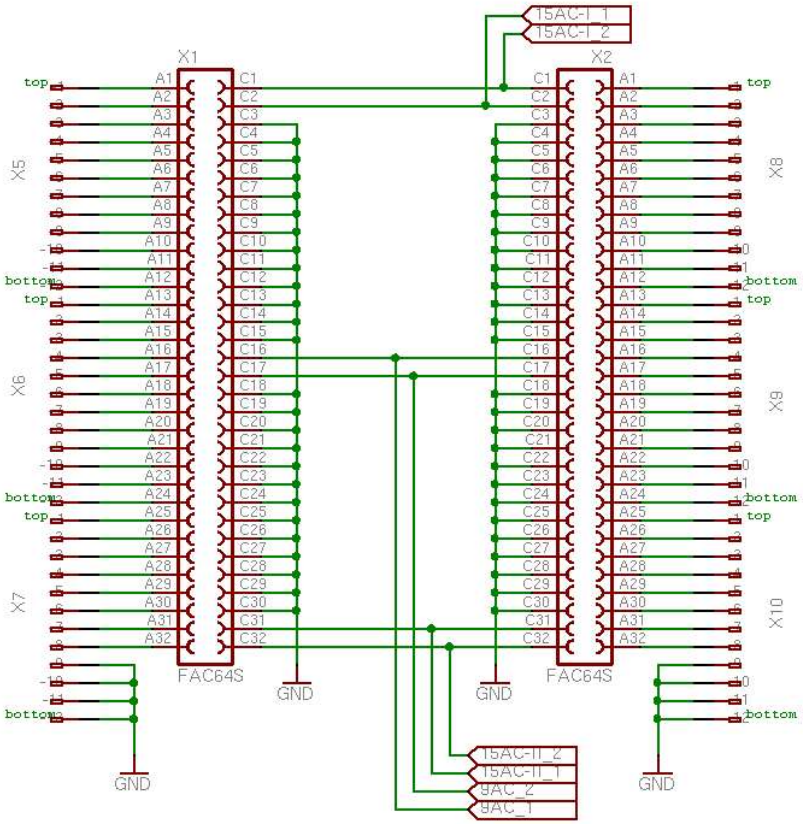
- L = Phase
- PE = Protection Earth
- N = Null.

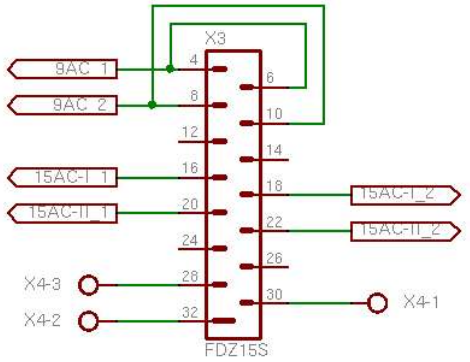
Interchanging this pin-out is not only dangerous, it can destroy the Viplax receivers or the power supply.

The terminals X5 to X10 carry the digital inputs and outputs of the Viplax receivers. The pin-outs of these terminals are shown in the printed circuit diagram for the Backplane Basic-Bi on the next page. For the Backplane Basic the terminals X1, X5, X6 and X7 are missing. The orientation of the connectors are shown in the printed circuit board as top and bottom. This is equivalent to the orientation in Figure 26. In the following table there is a summary of all connector pin-outs (X5 / X8; X6 / X9; X7 / X10).

Pin X6/8	***Signal***	***Pin X7/9***	***Signal***	***Pin X8/10***	***Signal***
1 (top)	A1	1 (top)	A13	1 (top)	A25
2	A2	2	A14	2	A26
3	A3	3	A15	3	A27
4	A4	4	A16	4	A28
5	A5	5	A17	5	A29
6	A6	6	A18	6	A30
7	A7	7	A19	7	A31
8	A8	8	A20	8	A32
9	A9	9	A21	9	GND
10	A10	10	A22	10	GND
11	A11	11	A23	11	GND
12 (bottom)	A12	12 (bottom)	A24	12 (bottom)	GND

Table 20: Pin-out of the Terminals X5 to X10 of the Backplane.





Inventronik GmbH, 2004 Backplane Basic-Bi		
TITLE: backplane_basic-bi		
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Repair

In case of a faulty component, please send the device along with an exact description of the error directly to Inventronik GmbH.